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EDN®

SPECIAL ISSUE:
Military electronics

Military relays

ECL-programmable gate arrays and PLDs

Troubleshooting analog circuits—Part 7

ELECTRONIC TECHNOLOGY FOR ENGINEERS AND ENGINEERING MANAGERS

Special Report
Real-time Ada

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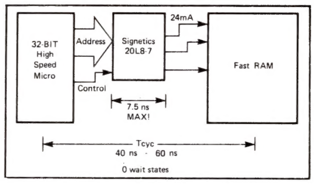
Turbocharge your memory for zero wait state design with Signetics fast 7.5ns PAL®-type devices.

Vroom! Now you can get the zero wait state performance that will allow memory to keep pace with the new ultra-fast microprocessors. And you won't have to pay top price for your memory to do it!



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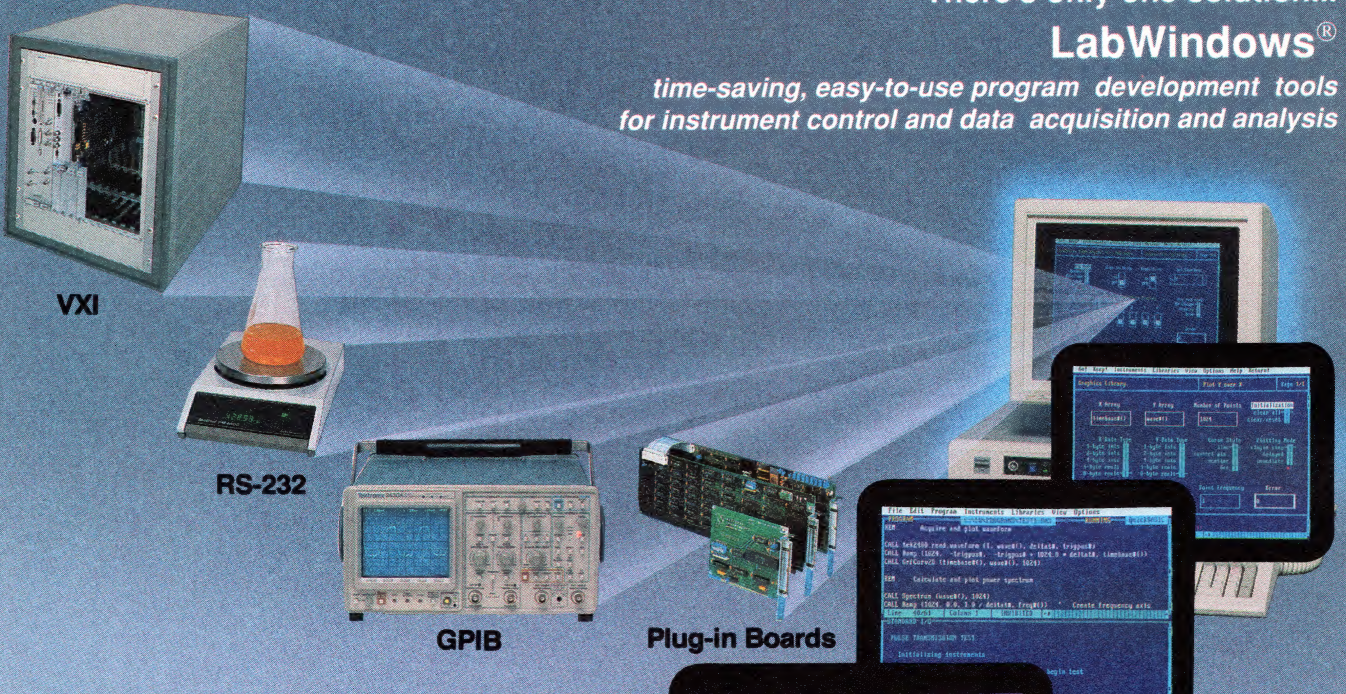

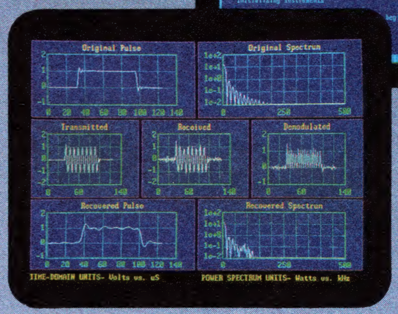

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CIRCLE NO. 2

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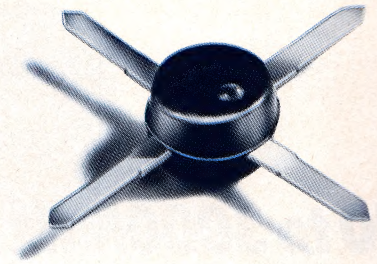


dc to 2000 MHz amplifier series

SPECIFICATIONS

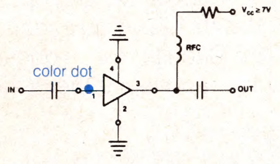
MODEL	FREQ. MHz	GAIN, dB 100 MHz	1000 MHz	2000 MHz	Min. (note)	• MAX. PWR. dBm	NF dB	PRICE $ Ea.	Qty.
MAR-1	DC-1000	18.5	15.5	—	13.0	0	5.0	0.99	(100)
MAR-2	DC-2000	13	12.5	11	8.5	+3	6.5	1.50	(25)
MAR-3	DC-2000	13	12.5	10.5	8.0	+8 □	6.0	1.70	(25)
MAR-4	DC-1000	8.2	8.0	—	7.0	+11	7.0	1.90	(25)
MAR-6	DC-2000	20	16	11	9	0	2.8	1.29	(25)
MAR-7	DC-2000	13.5	12.5	10.5	8.5	+3	5.0	1.90	(25)
MAR-8	DC-1000	33	23	—	19	+10	3.5	2.20	(25)

NOTE: Minimum gain at highest frequency point and over full temperature range.
• 1dB Gain Compression
□ +4dBm 1 to 2 GHz

designers amplifier kit, DAK-2

5 of each model, total 35 amplifiers

only $59.95



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*MAR-8, Input/Output Impedance is not 50ohms, see data sheet. Stable for source/load impedance VSWR less than 3:1

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80 × 50	10%	X7R	2200, 4700, 6800, 10,000 pf
120 × 60	10%	X7R	.022, .047, .068, .1μf

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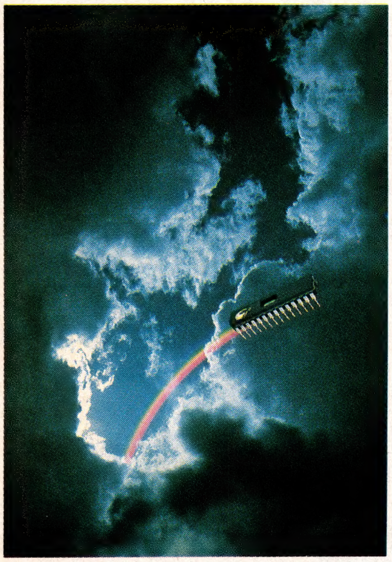
CIRCLE NO 16

EDN Magazine Edition®

Volume 34, Number 17 August 17, 1989

ELECTRONIC TECHNOLOGY FOR ENGINEERS AND ENGINEERING MANAGERS



On the cover: *Ada can make your real-time projects soar—whether they're military or commercial. See the Special Report, beginning on pg 102. (Photo courtesy Telesoft; art direction by Business Art)*

SPECIAL REPORT

DESIGN FEATURES

Continued on page 7

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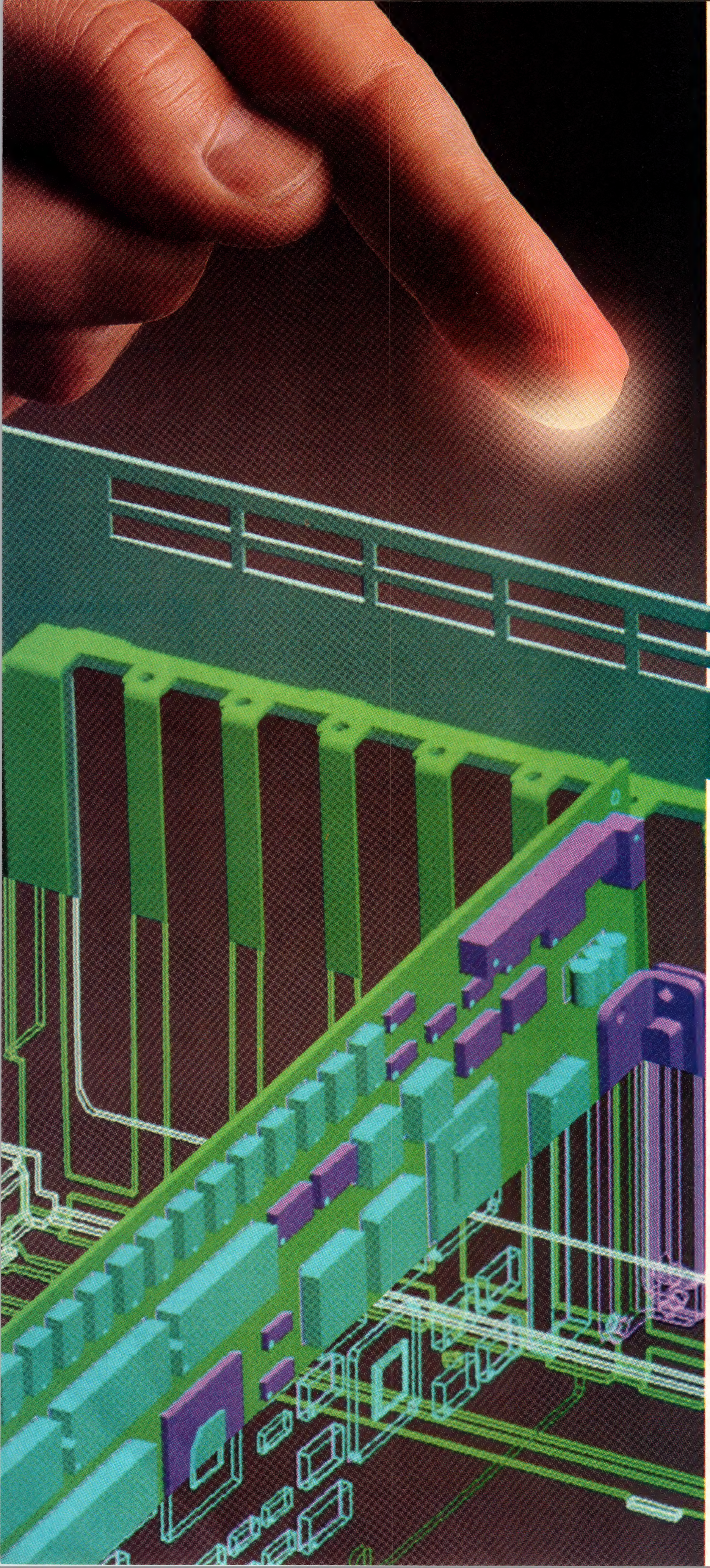

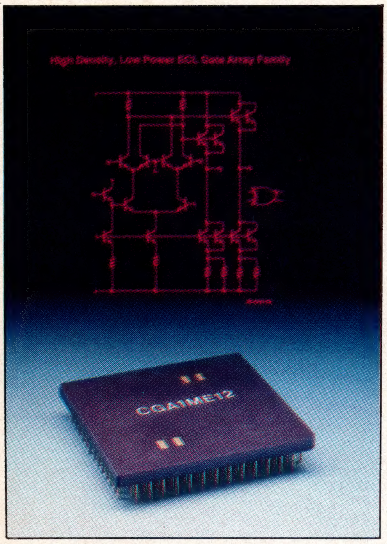

***You can choose** from a wide variety of ECL gate arrays and PLDs to solve your high-performance system needs (pg 73).*

Continued on page 9

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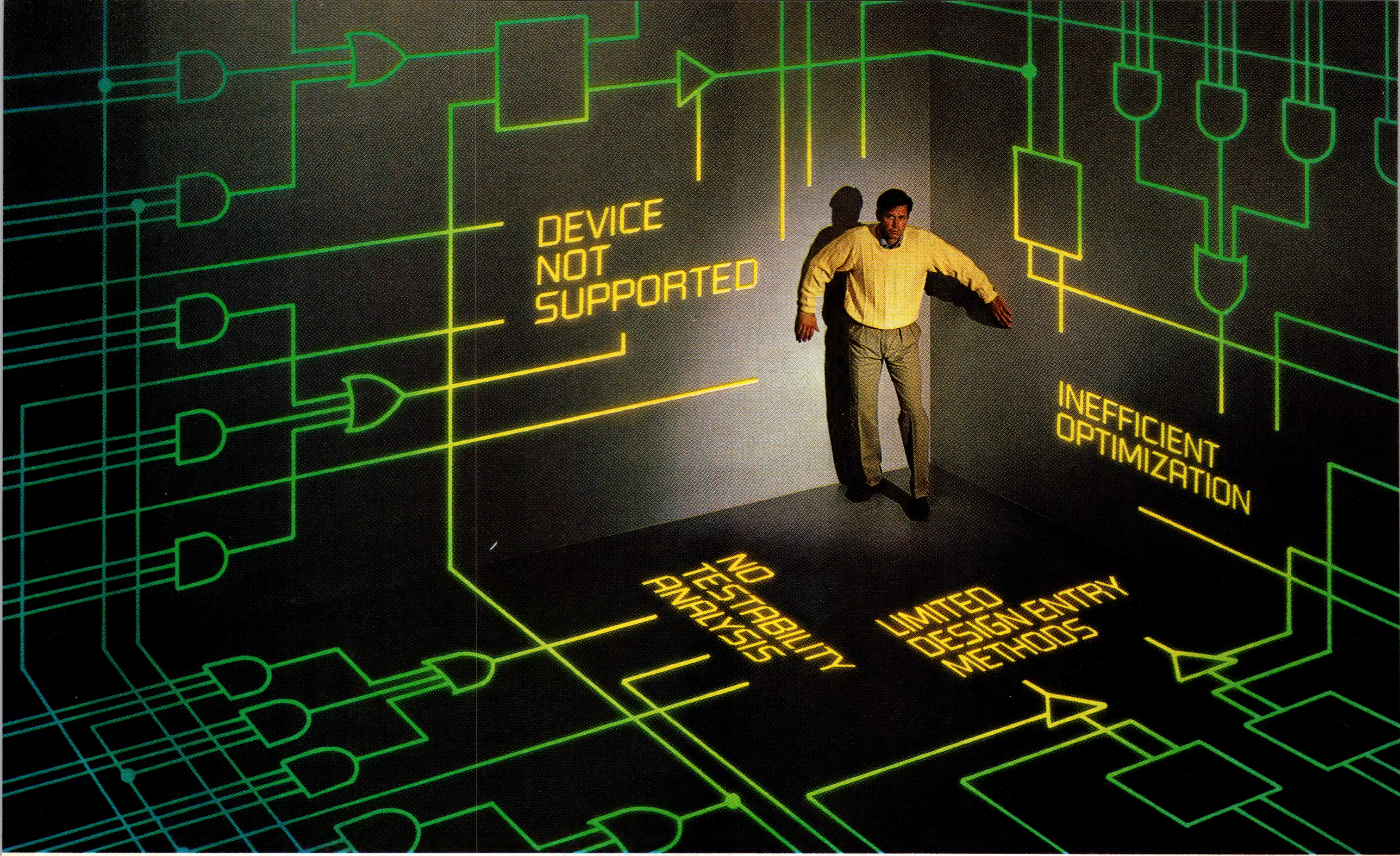

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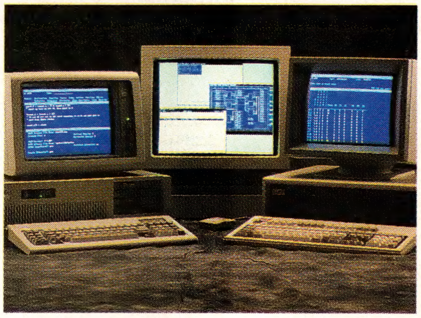

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CIRCLE NO 18

Continued from page 7

EDITORIAL

NEW PRODUCTS

DEPARTMENTS


64k×1
16k×4
16k×1
4k×4
16k×1
4k×4
8k×8
4k×1
1k×4
inmos
8k × 8
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Organisation	Part No.	Access Time
4K×1	IMS 1203	20,25,35,45
	IMS 1203M	25,35,45
1K×4	IMS 1223	20,25,35,45
	IMS 1223M	25,35,45
16K×1	IMS 1403	25,35,45,55
	IMS 1403M	35,45,55
	IMS 1403LM	35,45,55
	IMS 1400M	45,55,70
	MK41H67	20,25,35
4K×4	IMS 1423	25,35,45,55
	IMS 1423M	35,45,55
	IMS 1420M	55,70
	MK41H68	20,25,35
	MK41H69	20,25,35
	MK41H79	25,35
2K×8	MK6116	150,200

Organisation	Part No.	Access Time
2K×8	MK6116L	150,200
	MKI6116	150,200
	MKI6116L	150,200
64K×1	IMS 1600	20,30,35,45,55
	IMS 1601L	45,55
	IMS 1600M	45,55,70
	IMS1601LM	45,55,70
16K×4	IMS 1620	25,30,35,45,55
	IMS 1620M	45,55,70
	IMS 1620LM	45,55,70
	IMS 1624	25,30,35,45,55
	IMS 1624M	45,55,70
	IMS 1624LM	45,55,70
8K×8	**IMS 1630M**	**55,70**
	IMS 1630L	**45,55,70,100,120**
	MK48H64	**70,120**
	MK48H64L	**70,120**

Key: M – Mil-std-883C, L – Low Power. Available soon – a new 256K SRAM.

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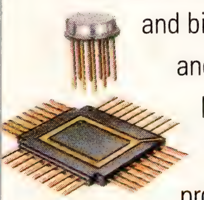

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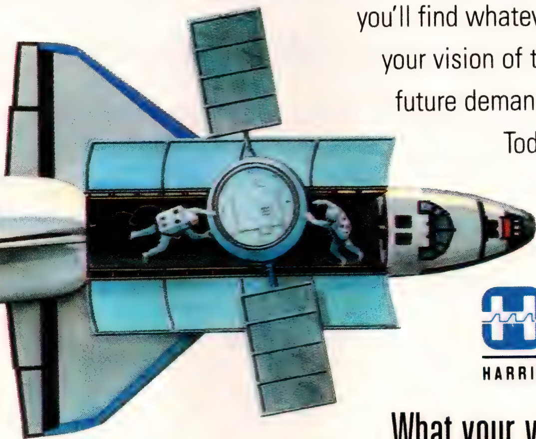

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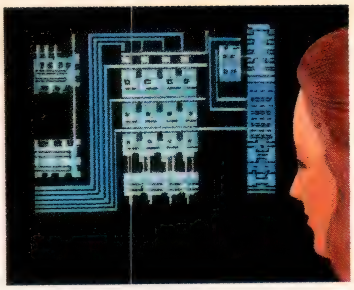

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CIRCLE NO 22

NEWS BREAKS

EDITED BY JULIE ANNE SCHOFIELD

INSTRUMENT-COMMAND SYNTAX TARGETS UNIVERSAL APPLICATION

Hewlett-Packard Co (Loveland, CO, (800) 752-0900) has announced that it will license an extensible instrument-command syntax called TMSL (test and measurement systems language). All of the company's VXIbus products and all rack-and-stack instruments it develops from now on will support TMSL. With the syntax, you issue the same command to obtain a measurement of, say, frequency, whether the instrument making the measurement is a counter/timer, a scope, or a spectrum analyzer and regardless of whether the instrument is a rack-and-stack unit or a VXI module. Thus, your instrument-control program is independent of the system hardware.

TMSL commands work in programs written in many high-level languages, including Basic, C, and Pascal. HP's Interactive Test Generator software generates commands in TMSL syntax when creating programs to control instruments that support TMSL. You can transmit TMSL commands over the IEEE-488 bus and over LANs. The book *TMSL syntactic and semantic requirements* and a license to use TMSL in your own designs and extend it without HP's prior approval cost $100.—Dan Strassberg

DIGITAL POTENTIOMETER CHIP PERMITS REMOTE ADJUSTMENTS

Now you can adjust equipment settings in the field without even opening the enclosure by using a software-controllable, solid-state dual potentiometer introduced by Dallas Semiconductor (Dallas, TX, (214) 450-0400). The DS1267 is a low-power CMOS chip containing two 256-position potentiometers that you can stack for double precision. You change the resistance with digital signals, and you can control an unlimited number of daisy-chained potentiometers with three signal wires. Because the DS1267 contains no mechanical contacts, it induces no operational noise and has an unlimited life. Its digital operation lets you change settings without incrementation and monitor its settings via an on-chip register. The chip can withstand high surface-mount assembly temperatures and sells for $4.60 (100).—J D Mosley

TACTICAL RAD-HARD ICs OFFERED AT LOW PRICE PREMIUM

United Technologies Microelectronics Center (Colorado Springs, CO, (719) 594-8000) now offers many of its gate arrays and standard military ICs with guaranteed tactical radiation-hardness specs meeting MIL-M-38510 level M (3×10^3 rads (Si)) or level D (1×10^4 rads (Si)) for a price premium ranging from 5 to 10% over the cost of the equivalent, nonradiation-hard part. The company employs epitaxial wafers and silicon-gate CMOS structures to provide immunity to single-event upsets, transient upsets, and latch-up. Thus, the radiation hardness is built, not tested, into the company's tactically radiation-hard parts. UTMC fabricates these ICs using the same process controls it employs on its strategic radiation-hard IC manufacturing line. Low-temperature processing enhances the ICs' total-dose radiation immunity.

In the past, designers of military systems with tactical radiation-hard requirements, such as avionics, shipboard electronics, and ground-based communications systems, had only two choices. They either proved the radiation hardness of nonradiation-hard ICs by testing individual parts, or they overdesigned systems by using parts with strategic radiation-hard specs (1×10^6 rads (Si)). However, these design practices are prohibitively expensive. UTMC's pricing policy for tactically radiation-hard ICs is a third, less costly alternative.—Steven H Leibson

MULTIPROCESSOR DSP BOARD OFFERS 50-MIPS PERFORMANCE

The VE-32C-01V, 4-processor, VMEbus DSP board targets computationally intensive applications, such as image processing and graphics. Valley Enterprises Inc (Tamaqua, PA, (717) 668-3737) offers the board, which is based on AT&T Technology Systems' (Allentown, PA, (800) 372-2447) DSP32C processor. The board achieves peak performance specs of 50 MIPS and 100M flops. The DSP32C DSP μP includes 1536 32-bit words of on-chip RAM; the board includes an additional 32k to 128k bytes of static RAM per processor. Software support for the board includes an assembler, a linker, a simulator, and a compiler. The board also comes with a C language applications library that includes math, matrix-manipulation, signal-processing, image-processing, and graphics routines. The VE-32C-01V costs $7650 (10) with 32k bytes of RAM per processor.—Maury Wright

START-UP INTRODUCES LOW-COST FAULT SIMULATOR

Starting at $4500, the FasFault family of fault-simulation tools from Intrinsix Corp (Westboro, MA, (508) 836-4100) consists of C-based software programs and an IBM PC/AT-compatible plug-in board. Software that permits the use of the system as a network resource on other Unix workstations costs $3000. The lowest-cost version of the fault simulator evaluates designs with as many as 10,000 gates; a 25,000-gate version has a $3000 premium, and a 100,000-gate fault simulator will be available later this year. Intrinsix is committed to offering interfaces between FasFault and many popular software simulators; however, the Viewlogic Workview interface ($1500) is the only one now available.—Michael C Markowitz

FILE SERVER STORES 3 TERABYTES ON VHS CASSETTES

Honeywell's Test Instrument Div (Denver, CO, (303) 773-4581) fused its videotape-based VLDS data-storage peripheral and a tape-handling robot designed for broadcast-television studios to create the VLA 600, a network file server that connects to Ethernet LANs and stores more than 3T bytes (3 million megabytes) of data. The previously introduced VLDS tape drive stores 5.3G bytes on a VHS videocassette, and the VLA 600 accepts as many as five VLDS drives. When mounted in the tape-handling robot, the tape drive gains access to as many as 600 VHS cassettes, thus resulting in a capacity exceeding that of 18,000 reels of standard 6250-bpi, 9-track tape. Yet the VLA 600—which houses the VLDS drives, the tape-handling robot, and the videotape carousels—measures only 71×40×78 in. The unit's tape-handling robot can retrieve any cassette in 8 seconds or less. A VME chassis buried in the VLA 600 holds the electronics needed to operate the VLDS tape drives, control the robot, and manage LAN communications using the TCP/IP network-communications protocol. A VLA 600 with two VLDS drives costs $524,900.—Steven H Leibson

VMEBUS I/O CONTROLLERS TARGET SUN-COMPATIBLE MARKET

Interphase Corp (Dallas, TX, (214) 350-9000) offers five new VMEbus-based I/O controllers, including SCSI, IPI (Intelligent Peripheral Interface), and ESDI models. The boards can be used in any VMEbus applications, but are specifically designed for Sun Microsystems' (Mountain View, CA, (415) 960-1300) workstations. Models V/IPI 4460 (IPI-2 disk controller), V/ESDI 4401 (an ESDI controller with SCSI port), and V/SCSI 4410 (a single- or dual-channel SCSI adapter) all fit the 9U Sun-compatible VMEbus form factor. The boards cost $4850, $4195, and $3595, respectively. The $1295 V/Sun SCSI 3205 is a 6U direct replacement for Sun's SCSI-2 board. All of the controllers will be available this fall.—Maury Wright


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INTERFACE SCSI INSTRUMENTS TO YOUR SUN WORKSTATION

The SCSI488/S controller from IOtech Inc (Cleveland, OH, (216) 439-4091) lets you use the SCSI port on your Sun Microsystems (Mountain View, CA, (415) 960-1300) workstation to control IEEE-488 instruments and laboratory peripherals. The $1495 SCSI488/S doesn't occupy any of your workstation's slots, and any workstation connected via the Sun LAN can access IEEE-488 instruments connected to other workstations at any node on the network. The SCSI488/S comes with driver software for true multitasking, error-correction, and exception handling. You can write programs in any high-level language that controls Unix system services. For $2495 you can purchase the Sun version of DADiSP, a companion software package for waveform analysis and graphics.—J D Mosley

HALF-HEIGHT, 5¼-IN. HARD-DISK DRIVE STORES 500M BYTES

You can cram 500M bytes of data on the half-height Wren VI from Imprimis Technology Inc (Minneapolis, MN, (612) 936-6271). The $1560 (OEM qty) drive has an unformatted capacity of 502M bytes, incorporates an embedded-SCSI interface, and features a 16-msec average seek time. This new version of the Wren VI employs the company's patented zone-bit recording method to improve upon its predecessor, the 383M-byte Wren VI, which remains in production.—Steven H Leibson

ANALOG INTERFACE CHIP SIMPLIFIES SPEECH PROCESSING

If you need to improve the quality of speech produced by your cellular phone, wide-band audio, or speech-recognition circuit, investigate the TLC32044 analog-interface chip from Texas Instruments (Dallas, TX, (800) 232-3200). The TLC32044 provides a nominal bandwidth of 100 to 3800 Hz and incorporates a new receive-section filter with independently programmable roll-off points. The chip's transmit and receive filters' ripple is $\pm\frac{1}{4}$ dB; their measured delays are 250 and 300 μsec, respectively. The TLC32044 can perform onboard (sin x)/x frequency-response correction. Pricing begins at $19.45 (1000).—J D Mosley

PC/XT-COMPATIBLE LAN STATION SUITS EMBEDDED APPLICATIONS

The ST/16 IBM PC/XT-compatible computer module from PC-Office (San Diego, CA, (619) 268-3235) is based on the company's PC-Office LAN. The LAN station includes 768k bytes of RAM, a keyboard interface, a light-pen interface, and a power supply, yet its dimensions are only 4.7×1.8×6.4 in. The module incorporates the Intel (Santa Clara, CA, (408) 987-8080) 2×4-in. Wildcard-88 CPU board, which operates at 10 MHz. A half-length IBM PC/XT-compatible add-in slot lets OEMs configure the module for embedded applications, such as factory automation and point-of-sale terminals. The diskless station includes an interface to the PC-Office LAN and can boot from a remote Netbios node. The PC-Office LAN operates using a CSMA/CD communications protocol and can support data transfers as fast as 4M bps. OEM prices for the ST/16 range from $195 to $495.—Maury Wright

SCSI IC SUITS PC HOST-ADAPTER AND MOTHER-BOARD USES

The TMC-950 SCSI chip from Future Domain (Tustin, CA, (714) 259-0400) targets SCSI applications in personal computers. The IC includes the glue logic to interface with IBM-compatible PCs and essentially provide a single-chip SCSI implementation. You can use the IC directly on the mother board or on a host-bus-adapter board. The IC supports asynchronous SCSI data transfers as fast as 1.5M bytes/sec; in host-adapter applications, it can sustain transfers across the PC/AT bus at 9.6M bps. The TMC-950 costs $30.—Maury Wright

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AAA2800	60/70/80	256K x 1

*All series available in static column and page mode. SIMMS and SIPS available for each series.

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CIRCLE NO 24

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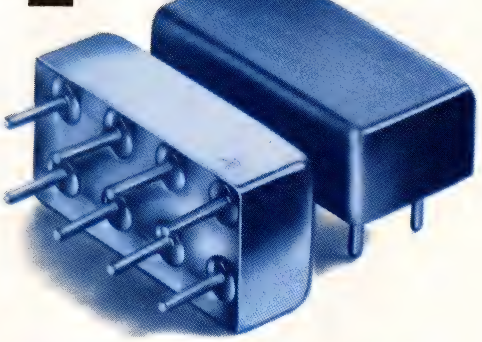

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MAN-1	0.5-500	28	1.0	8	4.5	60	13.95
MAN-2	0.5-1000	19	1.5	7	6.0	85	15.95
MAN-1LN	0.5-500	28	1.0	8	2.8	60	15.95
◇MAN-1HLN	10-500	10	0.8	15	3.7	70	15.95
*MAN-1AD	5.500	16	0.5	6	7.2	85	24.95

††Midband $10f_L$ to $f_{u/2}$, ±0.5dB †ldB Gain Compression ◇Case Height 0.3 In.
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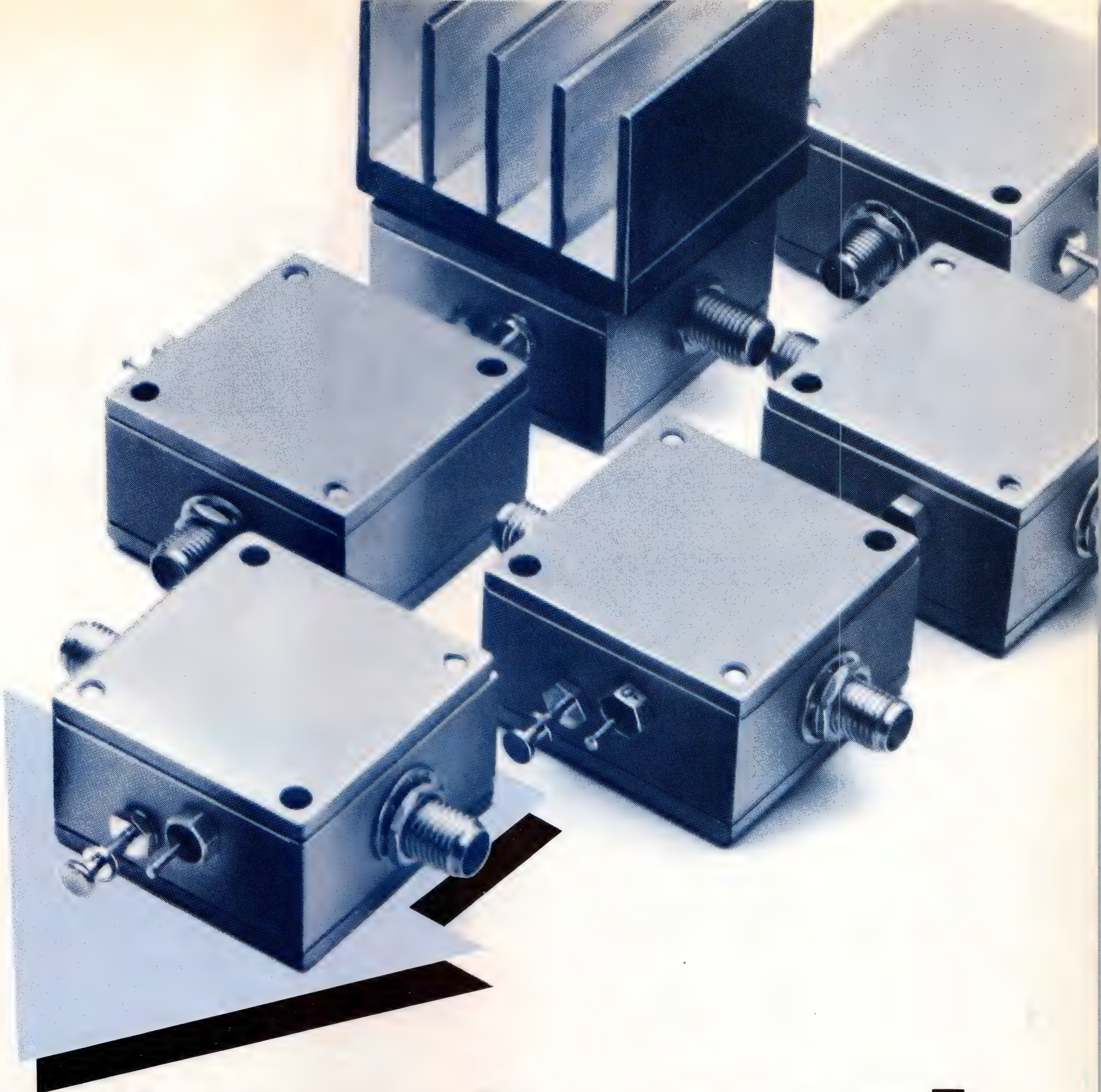

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MODEL	FREQUENCY MHz	GAIN, dB (min.)	MAX. POWER OUTPUT dBm(typ)	NF dB(typ)	PRICE $ Qty. (1-9) Ea.
ZFL-500	0.05-500	20	+9	5.3	69.95
ZFL-500LN	0.1-500	24	+5	2.9	79.95
ZFL-750	0.2-750	18	+9	6.0	74.95
ZFL-1000	0.1-1000	17	+9	6.0	79.95
ZFL-1000G*	10-1000	17	+3	12.0	199.00
ZFL-1000GH*	10-1200	24	+9	15.0	219.00
ZFL-1000H	10-1000	28	+20	5.0	219.00
ZFL-500HLN	10-500	19	+16	3.8	99.95
ZFL-1000LN	0.1-1000	20	+3	2.9	89.95
ZFL-1000VH	10-1000	20	+26	4.5	229.00
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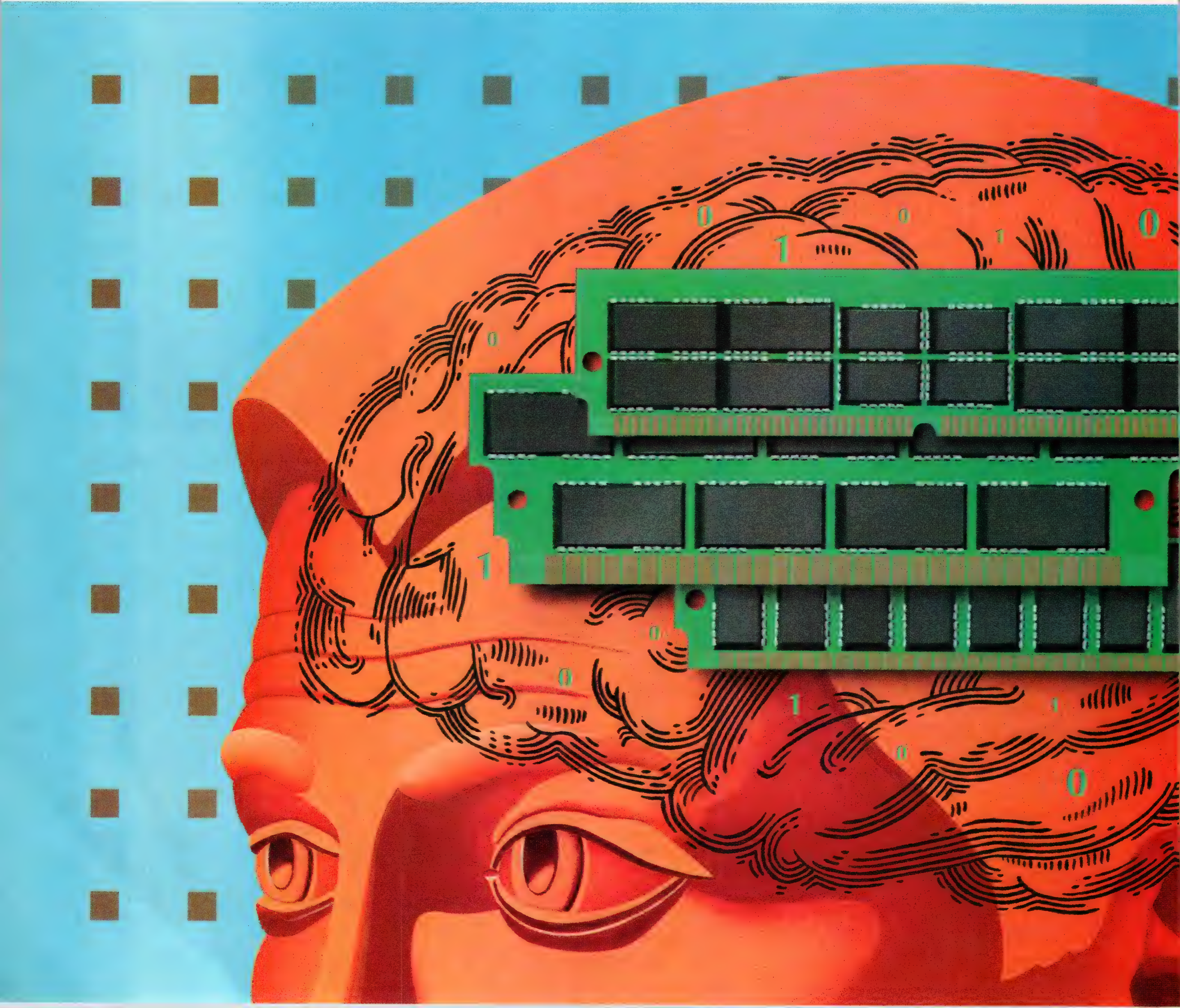

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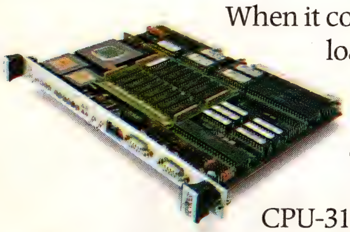

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SIGNALS & NOISE

Frequency affects output impedance

Sergio Franco proposes (EDN, June 8, 1989, pg 187) that you should compute the correct values for capacitors, such as 34.29 pF, because "empirical values do not necessarily guarantee optimum results." These values are supposed to give optimum results when you analyze an op-amp circuit in Spice. However, Mr Franco's analysis assumes that the output impedance of an op amp has a constant resistive value at all frequencies.

My data show that many op amps have low Z_{OUT} at moderate frequencies, but this Z_{OUT} can rise (inductively) at high frequencies. Some op amps start out with a high value of R_{OUT}, which falls (capacitively) to a lower value at high frequency. Because many op amps do not have a constant R_{OUT} at high frequencies, I find it necessary to breadboard and test the actual circuit rather than just trust that the computed values are correct, for the following reasons: An op amp's output impedance is not easy to express mathematically; makes the mathematical analysis quite messy; and tends to change value and thus affects the op amp's frequency response when the output changes from sourcing current to sinking current.

I do agree that Sergio's computations are a good place to start.

Robert A Pease
Staff Scientist
National Semiconductor
Santa Clara, CA

Pertinent points about PCPlot

Thank you for including PCPlot in the Technology Update "Draw your graphs on printers and plotters" (EDN, April 13, 1989, pg 53), which compared graphing-software packages. As PCPlot's author, I found the article informative and well written. Unfortunately, some errors occurred in the evaluation of PCPlot. It was stated that PCPlot "produces plots with as many as 1000 points." This is not true. PCPlot produces plots with as many as 6000 points and allows as many as six data files (1000 points per data file) to be plotted on the same graph. This capability is an important factor for engineers who plot more than one set of data on the same graph.

It also stated, "Unfortunately, BV Engineering's programs don't let you store graphic images in files for later use." Our Plotter Driver Program enables you to save images in the native language of the plotter that you select (HPGL, DMPL, etc). Since these are common graphic-image formats, BV Engineering's programs do indeed support this important feature.

It was our intention to create a graphing program that's easy to learn and use. In PCPlot, we have accomplished that goal. Even untrained, nontechnical people can learn to use PCPlot in a matter of minutes.

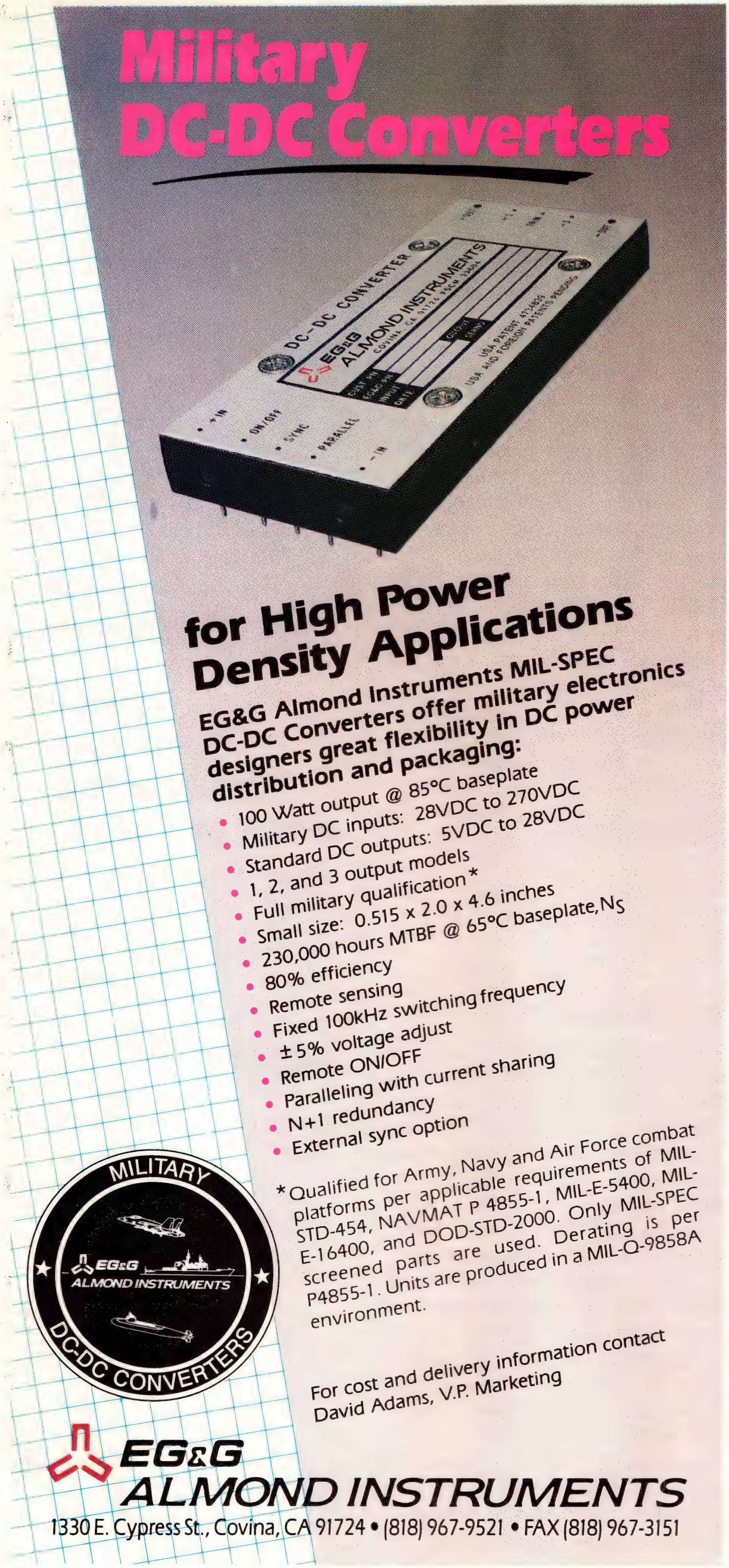
Steve Sauls
BV Engineering
Riverside, CA

Who "belongs" in the US?

One day this fellow who was working in our department said, "Why don't these foreigners go back where they came from?" (See Jon Titus's editorial, "Send alien graduates home," EDN, October 27, 1988, pg 57.) I asked him casually, "John, where did you come from?" He replied that he was born here.

I asked him where his parents came from. He replied that they came from Poland. Then I said, "Why don't they go back home?" He said they didn't like it back home. Life and things were tough.

I remember this dialogue with John vividly. I told him, "John, tell me in what sense you have contributed more than I have to this country? I am more educated than you.



SIGNALS & NOISE

I pay more taxes than you. I work harder than you. I teach and train. I don't smoke or drink. I don't sell or buy drugs. I am honest and more patriotic than you will ever be, because I know the value of freedom. I know the value of free expression. I will never sell the secrets of this country, and I will never pollute, destroy, or deface any part of this country. I will never belittle, disgrace, or expose any weakness of this country. This is one of the few countries where we, the people, can make it stronger. In most countries, this right is usurped by a few. I am thankful that I have the opportunity to be here and contribute in whatever fashion I can. I am very proud to be a naturalized citizen of the United States."

John said he never thought of it that way. Later, we became good friends.

I cannot say this about Jon Titus. I believe, however, he has been enlightened by the letters of Bill Geary and Mike Lynn (Signals & Noise, EDN, May 25, 1989, pg 33). Well done, Bill and Mike.

M Kamal Khan
National Semiconductor
South Portland, ME

Missing phone numbers

In the Technology Update, "Software tools handle all µP traffic" (EDN, June 8, 1989, pg 89), the following phone numbers were inadvertently overlooked: (800) 245-6717 for PC-SIG in Sunnyvale, CA; and (206) 641-7978 for the Library Bulletin Board System in Seattle, WA.

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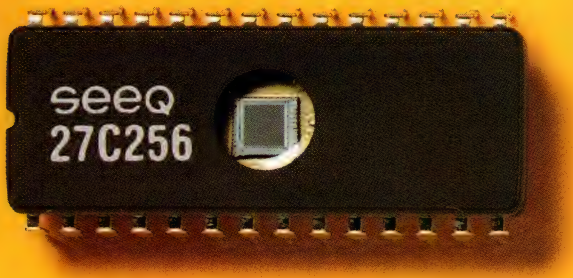

The memory density of a UVEPROM.

In a device that's priced at a fraction of the cost of EEPROMs.

It's the new FLASH EEPROM from SEEQ. And along with high density and low cost, it delivers the same kind of flexibility you need to get your design created. And implemented.

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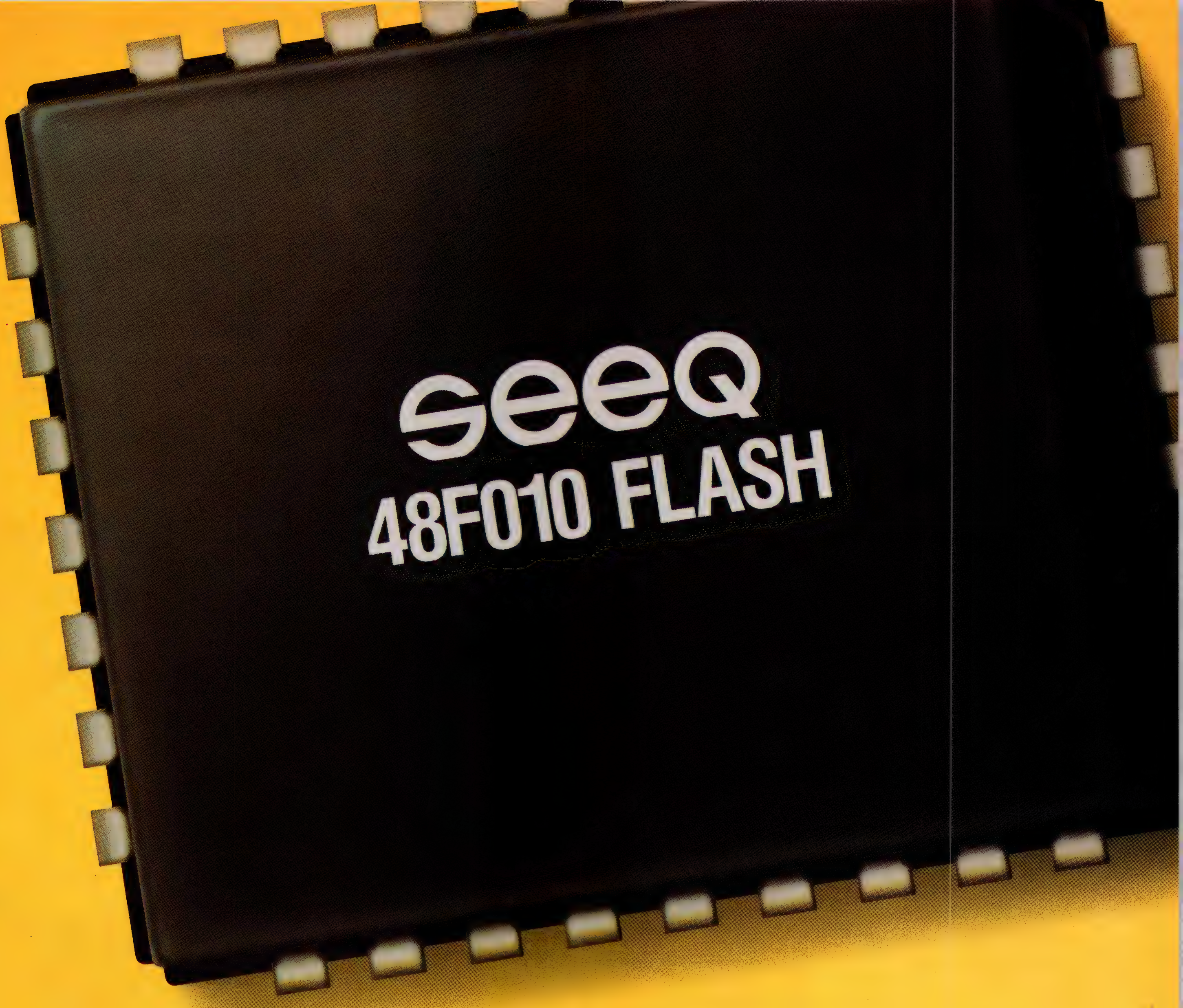
You can get our 1Mb FLASH in ceramic and plastic surface mount packages, as well as both plastic and

The electrical erasure of an EEPROM.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Switch to the leader in POWER MOSFET isolated package technology, SGS-THOMSON Microelectronics, from day one you'll get isolated power that will help blast you right past your competition.
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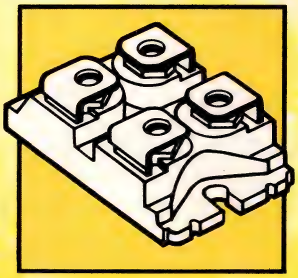
- One device replaces 4 or 5 standard devices



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Data Communication Concepts (seminar), Los Angeles, CA. Technology Transfer Institute, 741 10th St, Santa Monica, CA 90402. (213) 394-8305. August 23 to 25.

11th Quartz Devices Conference and Exhibition, Kansas City, MO. Electronic Industries Association, 1722 Eye St NW, Washington, DC 20006. (202) 457-4981. August 28 to 31.

International Test Conference 1989, Washington, DC. International Test Conference, Box 264, Mt Freedom, NJ 07970. (201) 895-5260. FAX 201-895-7265. August 29 to 31.

Surface Mount '89, San Jose, CA. MG Expositions Group, 1050 Commonwealth Ave, Boston, MA 02215. (800) 223-7126; in MA, (617) 232-3976. August 29 to 31.

Real-time Structured Analysis & Design (short course), Washington, DC. John Valenti, Integrated Computer Systems, 6053 W Century Blvd, Los Angeles, CA 90045. (800) 421-8166; in CA, (213) 417-9700. FAX 213-410-2952. August 29 to September 1.

Midcon/89, Rosemont, IL. Midcon/89, 8110 Airport Blvd, Los Angeles, CA 90045. (213) 772-2965. September 12 to 14.

Aerospace & Electronics '89 (conference), Santa Clara, CA. National Computer Graphics Association, 2722 Merrilee Dr, Suite 200, Fairfax, VA 22031. (703) 698-9600. FAX 703-560-2752. September 12 to 15.

1989 Annual Conference of the International Federation of Consulting Engineers, Washington, DC. Jeanne Quick, American Consulting Engineers Council, 1015 15th St NW, Washington, DC 20005. (202) 347-7474. September 24 to 27.

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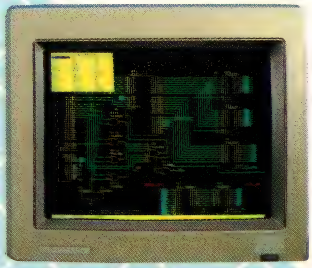

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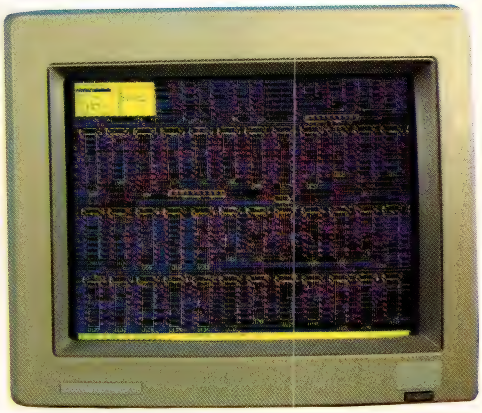

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CIRCLE NO 37

CALENDAR

Expo SMT International, Las Vegas, NV. Expo SMT, Box 1869, Los Gatos, CA 95031. (408) 354-0700. FAX 408-354-1036. September 25 to 27.

Diskcon, San Jose, CA. Julie Sunseri, 710 Lakeway, Suite 170, Sunnyvale, CA 94086. (408) 720-9352. FAX 408-736-2523. September 26 to 27.

IEEE International Conference on Computer Design (ICCD '89), Cambridge, MA. Giovanni De Micheli, Center for Integrated Systems, Room 129, Stanford University, Stanford, CA 94305. (415) 725-3632. October 2 to 4.

Electronic Imaging Conference East, Boston MA. MG Expositions Group, 1050 Commonwealth Ave, Boston, MA 02215. (800) 223-7126; in MA, (617) 232-3976. October 2 to 5.

20th Korea Electronics Show, Seoul, Korea. Joseph Burke, US Department of Commerce, Washington, DC 20230. (202) 377-5014. October 7 to 12.

Systems 89, Munich, West Germany. Gerald Kallman, Kallman Associates, 5 Maple Ct, Ridgewood, NJ 07450. (201) 652-7070. FAX 201-652-3898. October 16 to 20.

Northcon/89, Portland, OR. Northcon/89, 8110 Airport Blvd, Los Angeles, CA 90045. (213) 772-2965. October 17 to 19.

Supercomputing World, San Francisco, CA. MG Expositions Group, 1050 Commonwealth Ave, Boston, MA 02215. (800) 223-7126; in MA, (617) 232-3976. October 17 to 20.

Unix Expo '89, New York, NY. National Expositions Company, 15 W 39th St, New York, NY 10018. (212) 391-9111. FAX 212-819-0755. November 1 to 3.

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CIRCLE NO 38


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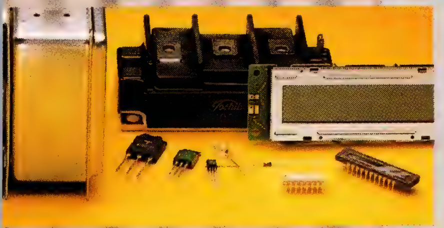

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Awakening the giant

The quotation, "I fear that all we have done is to awaken a sleeping giant," is attributed to Admiral Isoroku Yamamoto, who led the Imperial Navy's attack on Pearl Harbor in 1941. How times change. Now, many members of Congress, along with leaders of aerospace and electronics industries, should be applying the quote to the Japanese. The recent debate surrounding the licensing of technology to Japan for the coproduction of the FSX fighter plane may be having the opposite effect of what US industries want.

Instead of restricting the flow of technology to Japan, the FSX agreement may now push the Japanese to develop their own military systems—without sharing their technology with the US. When Japan expressed interest in working with the US on the FSX project, the US Department of Defense thought that the project would be mutually beneficial. Japan would gain a much-needed fighter aircraft, and US companies would gain from Japanese production subcontracts. However, some critics suspected that the Japanese would not give US companies a "reasonable" share of contracts.

Also, recalling the sale of advanced milling machines to the USSR, some people charged that Japan could not be trusted to keep the military technology out of enemy hands. People such as former trade negotiator Clyde Prestowitz, Jr, worried that Japanese industries might adopt US technologies shared under the FSX program and use them to establish an indigenous aircraft industry—in competition with US aircraft manufacturers.

The Japanese may have wearied of the debate over the FSX project. Recently, an influential Japanese business group, the Keidanren, suggested that it was time for Japan to double the country's military research and development budget. In fact, senior Japanese military and government officials think that the US will start withholding critical technologies—particularly those with both military and civilian uses. Thus, instead of working on an equitable technology-transfer arrangement, we're pushing the Japanese to start developing their own technologies—technologies in which the US won't share.

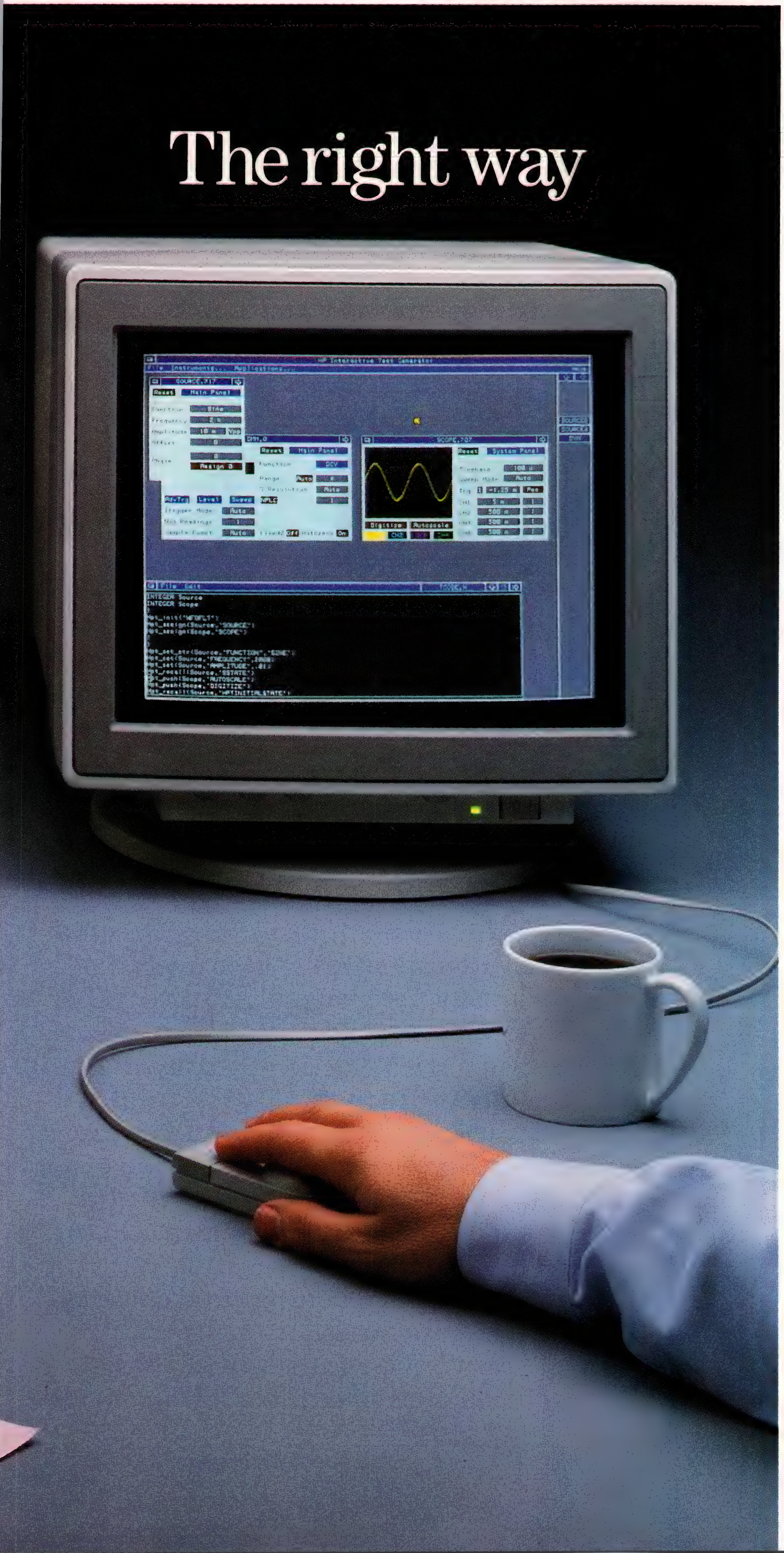
The US electronics industry should learn a lesson from the FSX debacle. It is often better to work with foreign companies and establish relationships based on mutual trust and respect; to build relationships that work to each participant's benefit. For example, in the microprocessor arena there are several vendors—among them Intel and Motorola—that do not yet have second sources for their advanced microprocessors. Those companies seem unwilling to license their µP technologies to domestic or foreign companies. Intel's arrangement with IBM is an exception. We doubt that IBM would continue to use Intel µP chips in its personal computers unless it had an agreement to make Intel-designed µP chips in IBM facilities.

Eventually, buyers will rebel at such technology or chip monopolies unless suppliers offer cross-license agreements. Such agreements don't always work out perfectly, but they seem preferable to adversarial sparring that turns customers and potential partners into direct competitors.

Jon Titus
Editor

Jesse H Neal
Editorial Achievement Awards
1987, 1981 (2), 1978 (2),
1977, 1976, 1975
American Society of
Business Press Editors Award
1988, 1983, 1981

Test development today:



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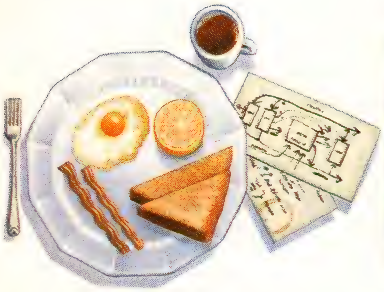
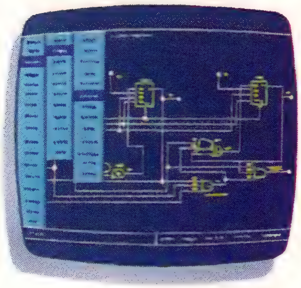
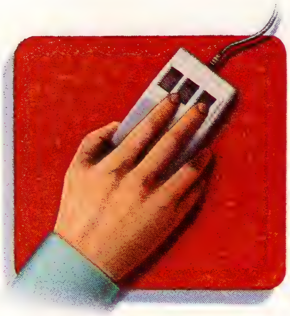


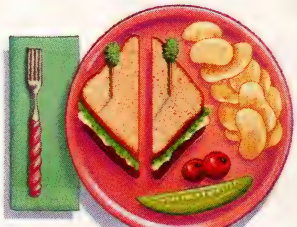
7:05 am : Breakfast
Suddenly, between bites, the answer to that new system design jumps right into your brain. But how to make it work in silicon? Use an Actel field programmable gate array!



8:50 am : Design
You warm up the design program on your 386 and put in the final touches. Then a quick rule check and 25 MHz system simulation with the Action Logic System software.



11:00 am : Place & Route
You watch the system place and route all 1700 gates (out of 2000 available) in under 40 minutes. 100% automatically! A final timing check. Then think of something to do until lunch.



12:00 pm : Lunch
Remember lunch? Normal people actually *stop working* and have a nice meal—right in the middle of the day! With Actel's logic solution, this could become a habit.

ACTEL FIELD PROGRAMMABLE GATE ARRAYS

They're a feast for your imagination.

Actel's ACT™ 1 arrays bring you a completely new approach to logic integration. Not just another brand of EPLD, PAL®, or LCA™ chips. But true, high density, desktop configurable, channeled gate arrays.

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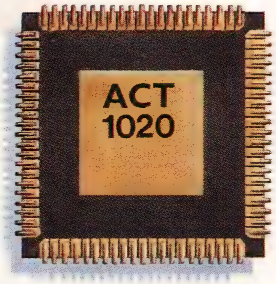
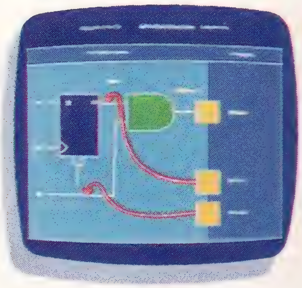
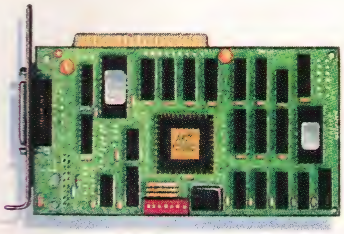
And do it in hours instead of weeks. Even between meals.

How? With features like 85% gate utilization. Guaranteed. Plus 100% automatic

Breakfast And
n By Dinner.







1:15 pm : Program
You load the Activator™ programming module with a 2000-gate ACT 1020 chip and hit "configure." Take a very quick coffee break while your design becomes a reality.

1:25 pm : Test
You do a complete, real-time performance check, with built-in test circuits that provide 100% observability of all on-chip functions. *Without* generating any test vectors.

4:00 pm : Production
Your pride and joy is designed, created, tested, and off to the boys in Production. And you're finished *way* ahead of schedule! Better think of something to do until 5:00.

6:00 pm : Dinner
Remember dinner? Normal people actually *go home* and eat with their families. On your way, start thinking about how Actel's logic solution can help you be brilliant tomorrow.

placement and routing. Guaranteed. So you finish fast, and never get stuck doing the most tedious part of the job by hand. And design verification is quick and easy, with on-chip Actionprobes™ that work with your logic analyzer to provide 100% observability of internal logic signals. Guaranteed.

All this is made possible by Actel's invention of the revolutionary PLICE™ antifuse programming element. Developed specifically for logic integration, PLICE antifuses and Actel's gate array architecture let you pack more functionality into much smaller spaces. No more splitting equations across multiple PLDs. Or being short on flip flops. Or running out of connections halfway through routing.

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It could make your whole day.

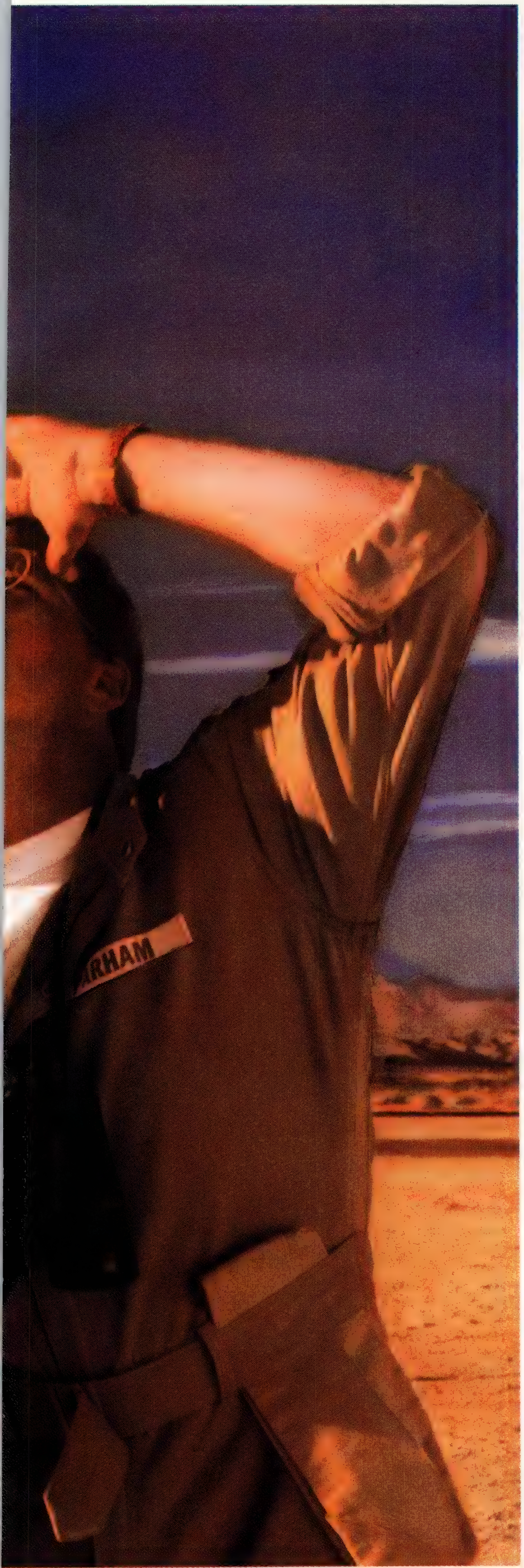
Actel

CIRCLE NO 15

Who was the second person

Captain James Fitzgerald was the second person to break the sound barrier at Muroc Dry Lake, on February 24, 1948.

to break the sound barrier?



Someone worked every bit as hard as Chuck Yeager and came in second. The sad truth is, no matter how fast you go, getting there second isn't fast enough.

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CIRCLE NO 14

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MILITARY RELAYS

Devices let aircraft use higher voltages

The electronic subsystems for tomorrow's aircraft will derive their power from high-voltage dc power systems. Advanced military relays enable next-generation aircraft to use these higher dc voltages.

Margery Conner,
Regional Editor

Aircraft systems designers have long agreed that a high-voltage dc power system for aircraft would allow a significant reduction in size and weight from the current 28V dc, 115V, 3-phase, 400-Hz ac systems. They haven't been able to use a higher voltage, however, because the industry lacked devices that could switch current at the higher dc voltage. Today's military relays, however, can carry hundreds of amperes at hundreds of volts. Thanks to these recently improved relays, the next generation of military and commercial aircraft will undoubtedly have high-voltage dc power systems.

Aircraft design contracts are in the bidding stage now, and neither the government agencies nor the prime contractors will say exactly what the dc voltage standard for military aircraft will be. However, the voltage will probably be 270V dc, because many existing subsystems obtain 270V dc power by implementing a full-wave rectification of the present 3-phase, 115V ac power. You can easily make these existing subsystems compatible with next-generation aircraft by pulling out the rectification circuitry from the subsystem and using the aircraft's raw 270V dc power.

One advantage of using higher dc voltages in aircraft is that systems that operate at such voltages save on size and weight, and are therefore more power efficient. For example, 400-Hz military aircraft generators have approximately 75% power efficiency, and 270V-dc generators have 80% to 90% power efficiency.

Designers of military systems are reaping additional savings from the use of smaller-gauge wire with the lower currents that result from higher voltages, and by using smaller magnetic

***Next generation aircraft** like the Army's Light Helicopter Experimental (LHX) may well benefit from reduced electronic subsystem size and weight—designs made possible by the use of high-voltage dc power systems. (Artist's concept courtesy McDonnell Douglas/Bell Helicopter Textron)*

cores in both power supplies and actuating motors. The newly developed, high-torque, samarium cobalt, brushless dc motors, for example, are a low-weight alternative to the hydraulic actuators currently used on aircraft.

Weight and size efficiency aren't the only advantages of high-voltage dc power. A dc generator is much quieter than a 400-Hz, 115V ac generator. Therefore, the radar signature of an airplane that has a high-voltage dc power system is much smaller.

Advanced relays for high current

Nevertheless, the military can't enjoy these benefits of high-voltage dc power systems without using more advanced relays that can carry high current at such high voltages. In the past, the three types of relays—solid state, electromechanical, and a hybrid of the two—presented crippling problems for engineers who wished to use higher voltages. Solid-state relays couldn't handle high current, and electromechanical relays had arcing problems; hybrids offered the advantages as well as the potential problems of both. Improvements in process technology have made it possible for relays to handle high current at higher voltages, but you'll have to consider each relay type carefully to decide which is most suitable for your high-current switching needs.

Of the three relay types, solid-state relays have had the most trouble handling high current. They switch current quietly because they have no mechanical contacts to cause arcing, but their junction voltage drop dissipates so much heat that at currents higher than approximately 5A, the relay's heat sinks make the relay package too large to use.

The M33C-5NS from Teledyne Solid State is one of the few military-rated solid-state switches capable of switching current at 270V dc. This relay has a maximum continuous operating voltage of 270V dc at 1.8A with no heat sink, and it fits in a 0.8×1.4×0.25-in. package. Thus, it can dissipate 486W without a heat sink. That wattage is a lot of power for a solid-state device, but it's still not enough for many aircraft applications, which require a relay to come in a small package and yet handle hundreds of amperes. The M33C-5NS costs $326 (50).

Unlike solid-state relays, electromechanical relays excel at carrying high currents. Because electromechanical relay contacts are metal, they have virtually no voltage drop, and therefore they require no heat sinks. One disadvantage of electromechanical relays is that they arc across their contacts upon being opened or closed, unlike solid-state relays. The next generation of military aircraft will spend much of its time at altitudes higher than 50,000 ft. The low-pressure atmosphere at these high altitudes causes acute arcing problems.

Hybrid relays consist of an electromechanical relay shunted with a solid-state relay, in an attempt to combine the arcless operation of solid-state devices with the low power dissipation of electromechanical relays. In a traditional hybrid design, the power semiconductor performs all the switching, carrying the full current for only a few milliseconds before the main contact—the electromechanical relay—switches in. Therefore, the solid-state device makes and breaks the circuit, and the electromagnetic contacts carry steady-state current. The presence of the solid-state relay not only quenches the electromechanical arc, but also eliminates bounce erosion on the metal contacts.

Nevertheless, hybrid relays are no panacea for all switching problems. At currents higher than approximately 100A, the energy that the semiconductor must absorb to quench the arc may require heat sinks that would be too large to use.

RPCs provide intelligence

Eaton's Aerospace and Commercial Controls Division has developed a purely electromechanical switch called a remote power controller (RPC). An RPC is an intelligent relay. It does more than simply switch power to a subsystem: it also

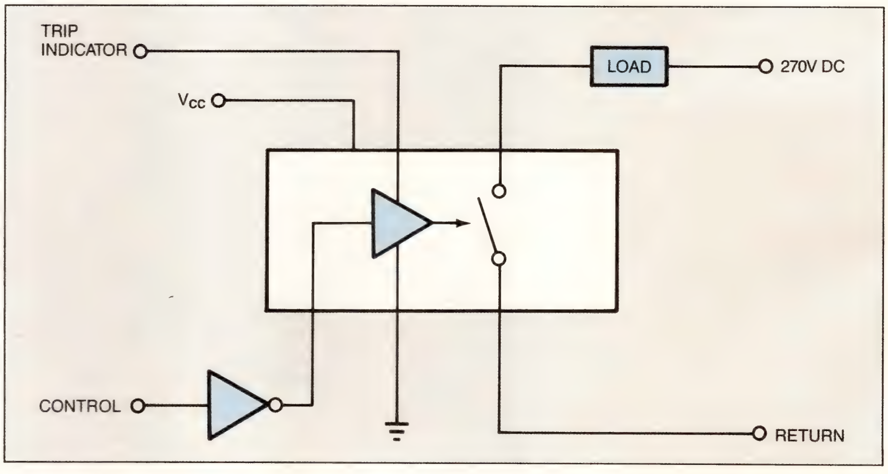

*Fig 1—**This simple solid-state relay,** the M33C-5NS from Teledyne Solid State, doesn't qualify as an RPC because it has the absolute minimum of status information—a trip indicator. However, for many low-current applications, a trip indicator provides all the status information you'll need.*

provides information about its status to a system computer. Common status information for an RPC is whether the relay is on or off, and why. Not all relays in next-generation aircraft will have to supply this degree of intelligence; notice that the Teledyne solid-state relay shown in **Fig 1**, which will be used in next-generation aircraft, provides only one status line.

Eaton's electromechanical RPC optically isolates its control logic from its power lines, to prevent noise on the power line from falsely triggering the control logic. If the environment is extremely noisy, and you wish to further isolate the RPC, you can power the relay from a separate power source other than the one the RPC is switching.

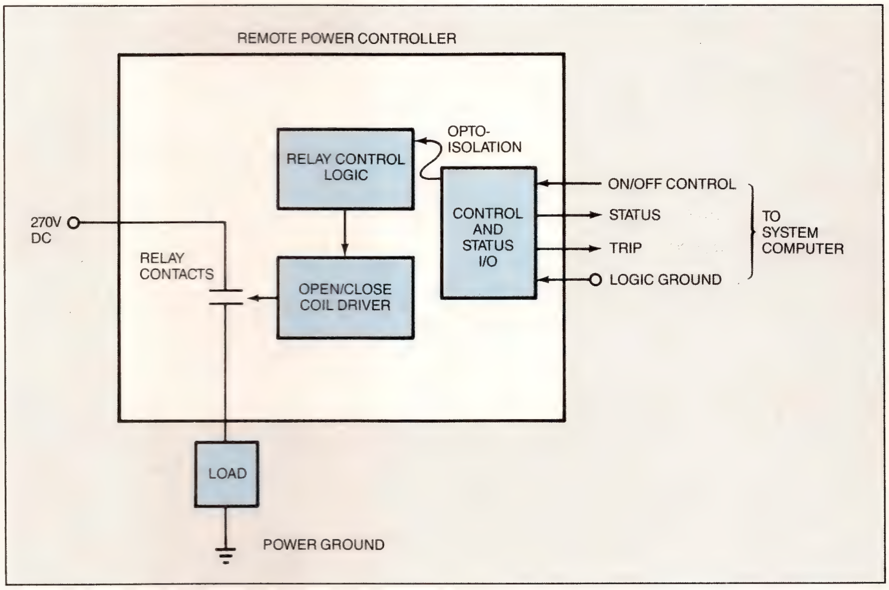

***Fig 2—An RPC can supply** extensive power-switch status information to the system computer. This electromechanical RPC features optoisolation of the control electronics from the power line and an arc-suppression chamber to extinguish the inevitable arc across the relay contacts. (Diagram courtesy Eaton Corp)*

Eaton's RPC is unique because it uses an arc-suppression chamber to extinguish arcing. It's impossible to eliminate an arc across an electromechanical relay's contacts when the circuit is broken, so the arc must be quenched one way or another. In a hybrid relay, the arc is fed through a semiconductor junction and dissipated as heat, but at very high currents (for example, greater than 100A), the semiconductor junction can't withstand the power surge of the arc and could blow apart. Eaton's electromechanical relay drives the arc off the relay's contacts to the arc-suppres-

"No military solid-state-relay market exists"

The best indicator of a viable market in electronic components is when several companies offer a catalog of standard parts, says Harvey Laner, vice president of marketing for Teledyne Solid State. Laner maintains that, by offering a catalog, a manufacturer signals that it can supply standard parts, often off the shelf. Until it has standard parts, a manufacturer can't take advantage of the economies of scale and the knowledge and refinements made possible by mass producing a standard part. In addition, when a company offers standard parts, designers gain confidence that the company can deliver the parts.

The Department of Defense (DoD) has vowed to standardize the parts it procures. Nevertheless, Laner points out that the government is still paying more for custom parts due to the current lack of standardization in the military solid-state-relay marketplace.

Laner offers several reasons for this lack of standardization in military solid-state relays. First, for several years, manufacturers have marketed solid-state relays as unique power-control units that must be custom ordered for each application. Sometimes this customization is necessary, but often it is not. As a result, engineers, not seeing parts readily available, create their own solid-state relays by taking a power FET, adding optical isolation and a logic-interfacing buffer stage, and ending up with a device that should have been available in a catalog in the first place.

Teledyne Solid State is now encouraging other manufacturers to make standard solid-state parts. Leach Relays, traditionally an RPC manufacturer, is seeking to enter the standard military-relay market by second sourcing Teledyne Solid State relays. Laner emphasizes that there can be no viable military solid-state-relay market until a good number of companies offer a catalog of standard parts.

Military relays

sion chamber, where the arc is broken down and extinguished. The arc is still there, but it can't ignite anything or be detected by radar.

Eaton's RPC fits into a 5×4.5×4.5-in. package. It's much bulkier than a solid-state device, but it doesn't require heat sinking. Each RPC costs approximately $2000, depending on the control circuitry.

A little-known alternative

Solid state, electromechanical, and hybrid relays are the traditional relay types with which everyone is familiar. But you should consider another, less well-known relay for your high-voltage, high-current switching needs: a type of electromechanical relay called a vacuum relay.

Vacuum relays are electromechanical relays whose contacts are enclosed in a vacuum. Because a vacuum relay has no gas molecules to ionize, no spark can jump across its metal contacts. Kilovac's KPC2 series of RPCs handles 15A without arcing or requiring heat sinks.

The size of Kilovac's vacuum relay is 3.25×1.5×2.2 in. The metal contactors are the only portion of the relay enclosed in a vacuum. Because the contactor gap is enclosed in a vacuum, the gap size is smaller than it would be under normal atmospheric conditions, and the relay's actuating coil shrinks to correspond to the smaller gap size (**Fig 3**). The relays cost approximately $1200 each. The basic contactor (AP 44A), which supplies no status information, costs $275.

These advanced relays are not only helping aircraft systems designers to attain their longtime goal of using higher dc voltages, but will benefit designers in the commercial sector as well. For example, the electronic subsystems of automobiles are also requiring ever-in-

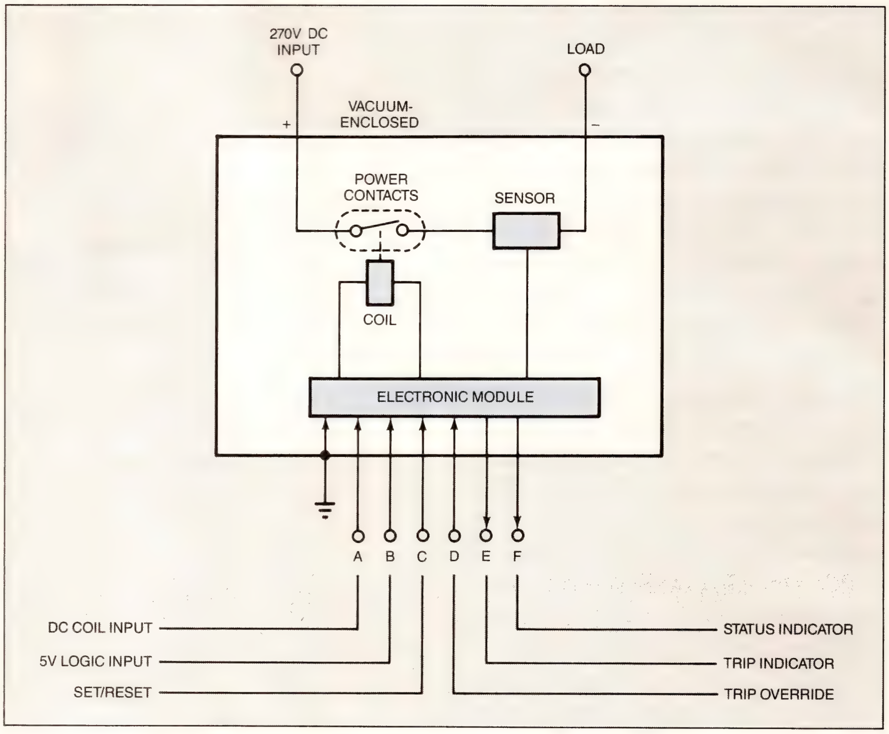

*Fig 3—**Only the relay contacts are enclosed in a vacuum** in the KPC2 RPC. Internal to the unit, the sensor monitors the open/closed status of the relay contacts and the status of the load, and it reports the status to the electronic module. Status Indicator reports the status of the power contacts, and Trip Indicator shows if the unit's maximum current has been exceeded. Unless the system computer activates Trip Override, the relay contacts open. Set/Reset clears the Trip Indicator signal. (Diagram courtesy Kilovac)*

For more information . . .

For more information on the military relays discussed in this article, circle the appropriate numbers on the Information Retrieval Service card or use EDN's Express Request service. When you contact any of the following manufacturers directly, please let them know you saw their products in EDN.

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creasing power. Designers of automobiles want to take advantage of the size and weight efficiencies offered by higher voltages. Consequently, within the next five years, you can expect to see a higher dc power system used in cars. Other commercial industries will also be demanding smaller, more lightweight switching controllers that can handle these higher voltages. EDN

Acknowledgement

The author wishes to thank Stan Schup, engineering group specialist with General Dynamics, for his help in researching this article.

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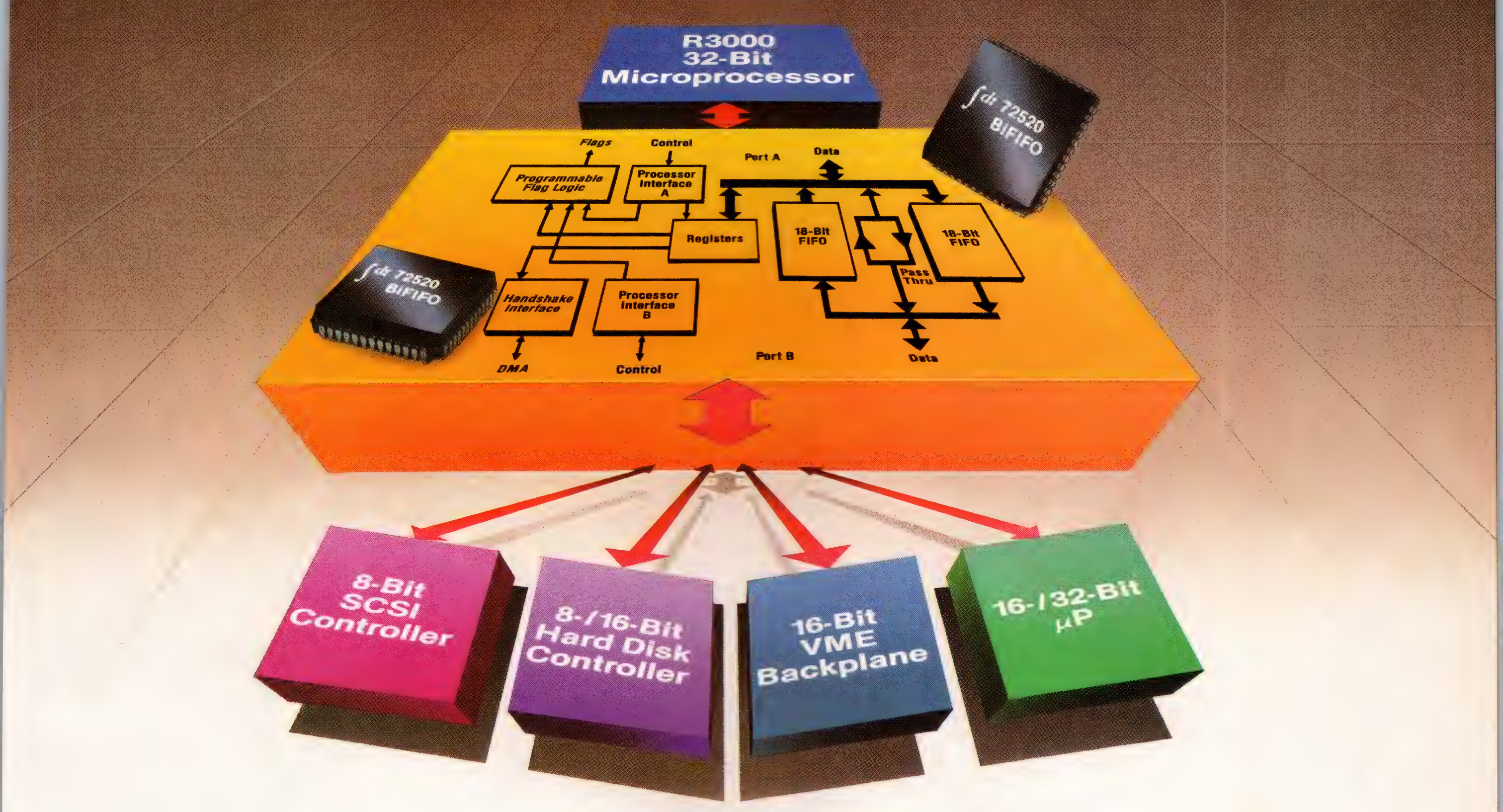
The μP-to-Peripheral Connection



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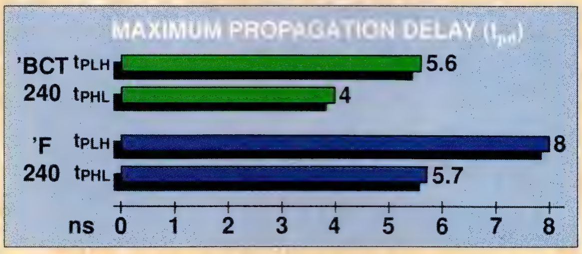

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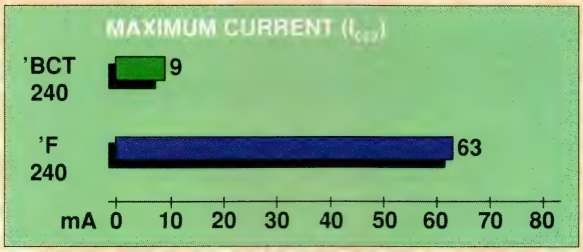

TI's power advantage: Here again, the BiCMOS driver wins over the advanced bipolar counterpart, exhibiting far less power dissipation.

be reduced as much as 95% (*see chart*) while active currents are cut as much as 50% compared to advanced bipolar equivalents.

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* David Shear, "EDN's advanced CMOS logic ground-bounce tests," *EDN*, Special Report, March 2, 1989.
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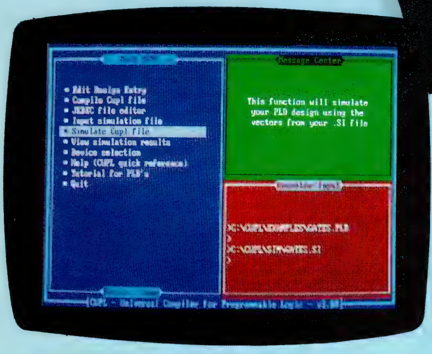

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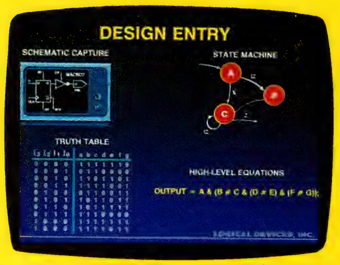

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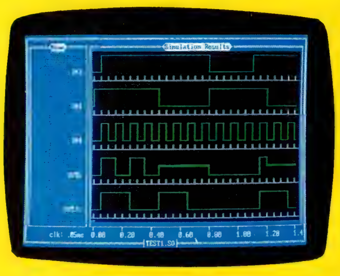

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MILITARY TECHNOLOGY

ECL GATE ARRAYS AND PLDs

ECL ICs play a role in high-speed computers

ECL gate arrays currently offer densities with CMOS complexities, and PLDs exist for "glueing" systems together.

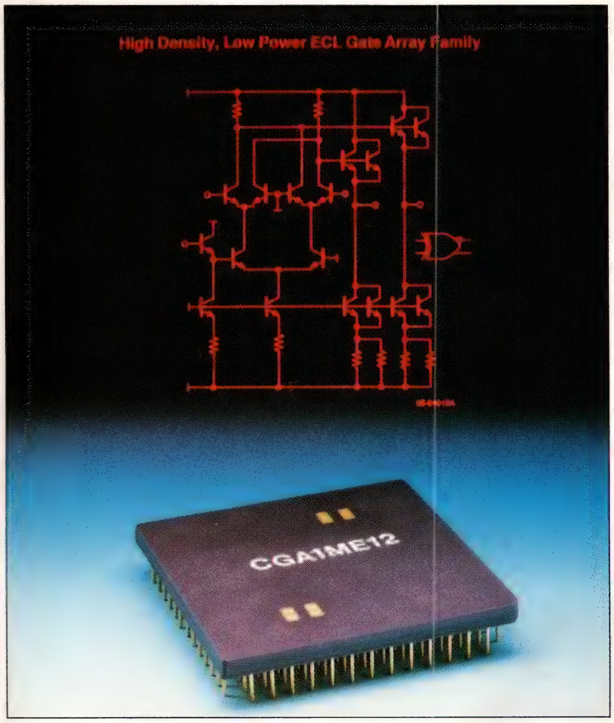
John Gallant,
Associate Editor

The never-ending quest for high performance in workstations, mainframes, ATE, telecommunications, and military systems mandates the use of high-speed, semicustom ASICs. System designers realize that LSI and MSI (medium-scale integration) offerings in the various logic families are inadequate for their needs. To fill this void CMOS, bipolar ECL, and GaAs vendors offer a variety of gate arrays and PLDs. Gate arrays satisfy applications requiring medium- to large-scale complexities, whereas PLDs are ideal for less complex designs. Each technology, however, has its pros and cons.

Current ECL gate arrays provide large-scale integration comparable to that of CMOS arrays, speed-for-power tradeoffs for thermal management, unloaded gate propagation delays of 300 psec or less, and cost and complexity advantages over their GaAs counterparts. Some recent interest in ECL gate arrays comes from Bipolar Technologies, which has produced an ECL version of Sun's SPARC processor, and Motorola, which has collaborated with Data General to transfer the 88000 reduced-instruction-set computer (RISC) CPU into ECL technology.

Even though BiCMOS and GaAs developments threaten ECL's overall market share, ECL does have a niche marketplace. Although bipolar ECL is synonymous with high speed, it is also synonymous with high power consumption. For this reason, a system designer must consider reliability, packaging, thermal management, and cost when evaluating the feasibility of an ECL design. The prudent designer only opts to use ECL over CMOS in applications requiring ECL's speed advantage. Because current CMOS gate arrays can reach into the 200-MHz-and-beyond range, an ECL gate array only becomes a viable option when an application requires frequency operation over 100 MHz.

ECL gate arrays must also compete



ECL gate arrays come in a variety of densities and speed options. *This Raytheon product specifies 4584 equivalent gates, has a 1.2-GHz D flip-flop toggle frequency, and a 1280-bit RAM cell.*

ECL-programmable gate arrays and PLDs

with GaAs gate arrays, which have made real inroads into the high-performance marketplace (**Ref 1**). By connecting enhancement- and depletion-mode (E/D) GaAs devices in a direct-coupled FET-logic configuration, GaAs products have flip-flop toggle rates greater than 1.5 GHz, and dissipate 0.2 to 0.4 mW per gate. A similar high-power ECL offering generally toggles less than 1.5 GHz, and dissipates from 1 to 2 mW per gate. Low-power versions dissipate from 0.5 to 1 mW per gate, but have lower toggle rates. However, current GaAs gate arrays are more expensive than ECL arrays for equivalent complexities. Although GaAs gate-array prices are rapidly decreasing, an ECL ASIC remains a cost-effective option for circuits operating below 1 GHz.

ECL manufacturers currently produce gate arrays with equivalent-gate densities greater than 10,000 gates per chip. For example, Advanced MicroCircuits Corp's (AMCC) Q20000 series and Siemens' SH100E series have family members with as many as 16,000 equivalent gates, and NEC recently introduced the μPB3000 family, which has as many as 35,000 equivalent gates. In addition, AT&T is about to introduce the BEST-I family, which will have as many as 20,000 equivalent gates, and Motorola plans to make its MCA-4 Series, a 50,000-equivalent-gate array, available in the first quarter of 1990. These large-complexity arrays minimize the number of off-chip interfaces, which can negate ECL's speed advantage. (**Table 1** offers a comparison of various ECL gate arrays.)

There is room for confusion when counting the number of equivalent gates for an ECL gate array, however. Gate counting is not as straightforward in ECL as it is in the other logic families. For example, CMOS gate arrays use the 2-input NAND gate as the basic unit for counting equivalent gates. Because the familiar 2-input CMOS NAND-gate topology requires four transistors, you merely have to count the number of transistors in the array and divide by 4 to arrive at an equivalent-gate count for the array.

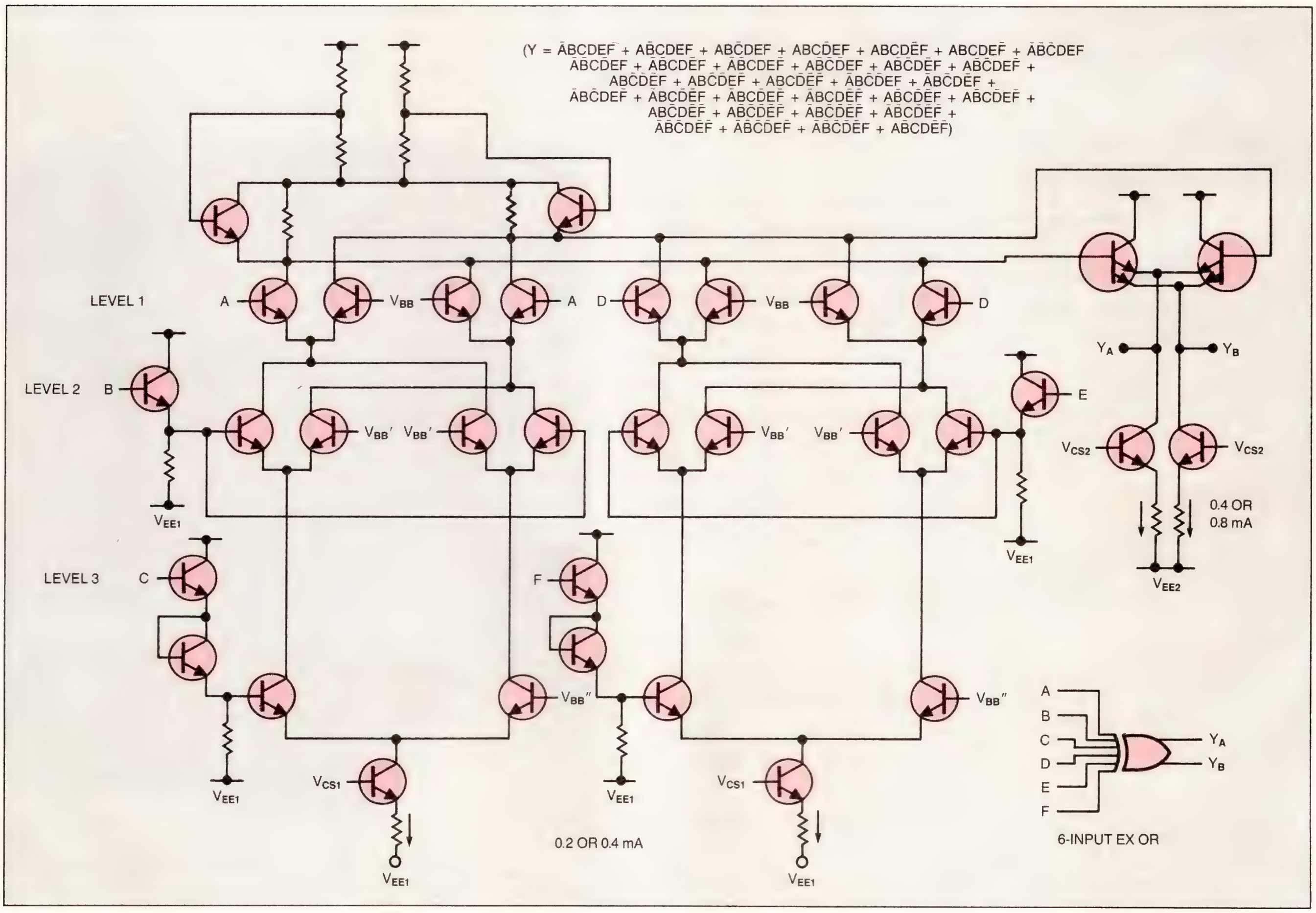


Fig 1—A schematic of a 6-input exclusive OR gate illustrates the gate economy that 3-level series gating provides. *This Motorola circuit uses three bias generators, V_{BB}, $V_{BB'}$, and $V_{BB''}$ as references for three gates operating from a single current switch.*

However, the current-mode-logic (CML) topology for ECL gives you a wide range of flexibility when you are configuring gates. Many vendors include three temperature-compensated, bias-voltage generators in the array, which can be used as reference voltages in a 3-level totem-pole arrangement known as series gating. The series-gate configuration operates from a single current source. An example of a 6-input-exclusive OR gate using 3-level ECL gating is shown in **Fig 1**. To implement this function with

TABLE 1—ECL GATE-ARRAY COMPARISONS

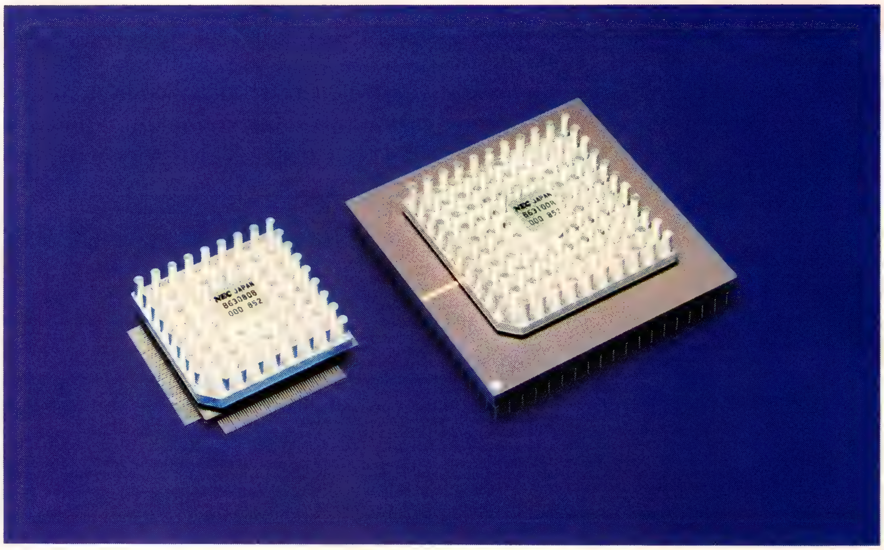
COMPANY	PRODUCT NAME	MAXIMUM NUMBER OF EQUIV-ALENT GATES	MAX-IMUM NUMBER OF I/O CELLS	UNLOADED GATE-PROPA-GATION DELAY (μSEC)	CHIP-POWER DISSI-PATION (MAX)	D FLIP-FLOP TOGGLE-RATE (MAX-IMUM) (GHz)	MAXIMUM NUMBER INTERNAL CELLS	GATE-EQUIVALENCY BASIS	COMPONENTS PER CELL	PACKAGE TYPES	COST	COMMENTS
AMCC	Q20000	16,000	256	120 140 190	16W	1.2	4274	D FLIP-FLOP W/RESET = 11 GATES = 3 CELLS	17 TRANSISTORS 17 RESISTORS	301PGA	$.05-$.07 PER GATE	MILITARY VERSION AVAILABLE, 3 METAL LAYERS TTL I/O
FUJITSU	H SERIES	9856	300	220 100	13W	1.0	1792	1 FULL ADDER = 11 GATES = 2 CELLS	16 TRANSISTORS 16 RESISTORS	208 PGA 260 FLAT PACK	$447 (1000) $461 (1000)	3 METAL LAYERS
	ET SERIES	6160	120	220	10W	0.80	1120	1 FULL ADDER = 11 GATES = 2 CELLS	16 TRANSISTORS 16 RESISTORS	149 PGA 164 FLAT PACK	$168 (1000) $177 (1000)	
	ET-M SERIES	3960	120	220	10W	0.80	720	1 FULL ADDER = 11 GATES = 2 CELLS	16 TRANSISTORS 16 RESISTORS	149 PGA	$217 (1k)	SERIES CONTAINS ARRAYS WITH RAM CELLS. 3 METAL LAYERS
	E128H	128	16	75	3W	4.0	32	D FLIP-FLOP = 4 GATES = 1 CELL		24 FLAT PACK	$330 (1000)	
MOTOROLA	MCA-3 SERIES	10,000+	256	120 300	6W	1.2	1656	MIXTURE OF D FLIP-FLOPS, OUTPUT LATCHES, AND INPUT ORS = 11,160 GATES	19 TRANSISTORS 19 RESISTORS	235PGA 289PGA 360TAB	$600 (100)	3 METAL LAYERS
	MCA-4 SERIES	50,000+	400	100 140 240	25W AND HIGHER	1.2	14,784	3.5 GATES = 1 CELL	19 TRANSISTORS 19 RESISTORS	550TAB	$1400 (100)	DESIGN-IN 1ST HALF OF 1990. 4 METAL LAYERS, ON-CHIP RAMCELL
NEC	ECL-4A SERIES	35,656	236	90 270	23.5W	1.4	3225	1 FULL ADDER = 11 GATES = 1 CELL		208PGA 280PGA 208QFP 280QFP	≈$750 (1000) ≈$890 (1000)	TTC I/O, 3 METAL LAYERS
	ECL-3B	11800	172	90	15W	0.3	1600	1 FULL ADDER = 11 GATES = 1 CELL		132PGA 208PGA	≈$270 (1000)	TTL I/O, 2-LEVEL GATING ONLY, 3 METAL LAYERS
RAYTHEON	70E18	12,800	176	300	5W	1.2	7696 MAPS	4 TO 1 MUX = 8 GATES = 5 MAPS	6 TRANSISTORS 6 RESISTORS PER MAP	232PGA	$460 (100)	TTL I/O, 2 METAL LAYERS. MILITARY VERSION AVAILABLE
	40E12	7,752	120	300	3,5W	1.2	4620 MAPS	4 TO 1 MUX = 8 GATES = 5 MAPS	6 TRANSISTORS 6 RESISTORS PER MAP	149PGA	$220 (100)	TTL I/O, 2 METAL LAYERS. MILITARY VERSION AVAILABLE
SIEMENS	SH100E SERIES	10,000	256	90	25W	1.5	2604	1 FULL ADDER = 11 GATES = 3 CELLS	10 TRANSISTORS 12 RESISTORS	319PGA 68LCC	$750 (100)	FAMILY CAN MIX ECL & CML LOGIC 3 METAL LAYERS, TTL I/O. MILITARY VERSION AVAILABLE
SONY	E3G200	200	34	150	1.7W	2.5	70	3 GATES = 1 CELL	14 TRANSISTORS 15 RESISTORS	24MFP 32MFP	$50 (1000)	2 METAL LAYERS 100KH LEVELS ONLY
	E3G70	70	48	>100	1.7W	3.5	70	3 GATES = 1 CELL	14 TRANSISTORS 15 RESISTORS	24MFP 32MFP	$50 (1000)	2 METAL LAYERS 100KH LEVELS ONLY

ECL-programmable gate arrays and PLDs

CMOS-equivalent gates would require 32, 6-input NAND gates and one 32-input OR gate.

In order to use 3-level series gating, you must provide a −5.2V supply to the chip. The large supply voltage provides an adequate margin for stacking the three reference generators, but requires either 10K or 10KH ECL-compatible voltage levels at the I/O ports. If you use a −4.5V supply, which makes the I/O ports compatible with 100K ECL voltage levels, you can only use 2 levels of series gating, thereby limiting the complexity of functions that you can design with a single current source.

Because of these anomalies, ECL gate-array vendors refer to their products as a sea of cells, rather than use the sea-of-gates terminology that applies to CMOS arrays. A cell consists of a number of transistors (typically 15 to 20) and resistors that can be configured into definable logic blocks by using macros from a cell library. The ECL array generally has an internal architecture consisting of columns of rows containing multiple cells. The bias-voltage generators are located at the end of each row. In addition, the ECL array has a number of I/O cells located around the chip's periphery.



Current ECL gate arrays offer large-scale integration densities comparable to their CMOS counterparts. *NEC's ECL-4A family has a member that exceeds 35,000 gates when the cells are fully populated as full adders.*

Gate counting tests your sanity

The ECL gate-array architecture contributes to the confusion when counting the number of equivalent gates. To arrive at a gates-per-cell number, vendors implement macros, such as a full adder or a D-type flip-flop, in one or more cells and count the number of logic gates implemented in a cell. This number is then multiplied by the number of cells in the array to arrive at an equivalent-gate count. The number of equivalent gates is not the same for each macro, however. For example, NEC calculates an equivalent-gate figure of 35,656 gates for its ECL-4A array when you arrange each cell as a full adder. The same device has an equivalent-gate count of 10,000 gates when fully populated with 2-input NAND gates.

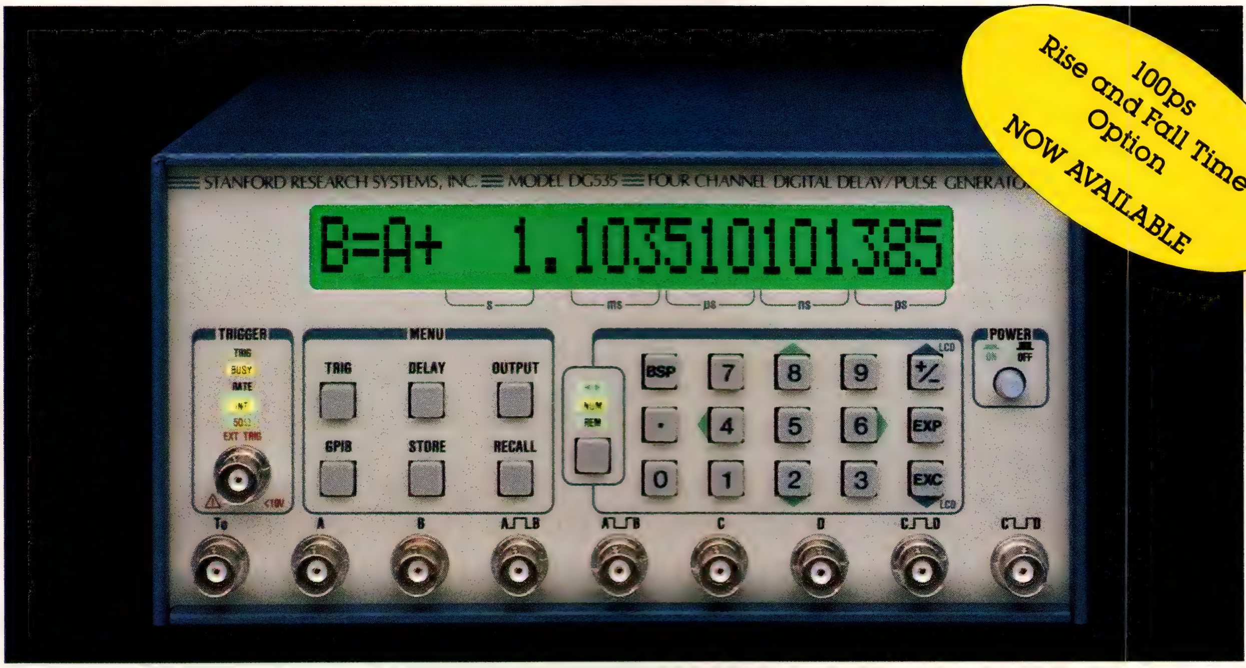
Furthermore, the number of equivalent gates per macro is not consistent among vendors. For example, AMCC implements a D flip-flop macro that uses 11 gates, whereas Raytheon's D flip-flop macro uses 7 gates, and Motorola's uses 9 gates. To further confuse matters, vendors often use the I/O cells for implementing macros. Because a typical application uses a variety of different macros, the equivalent-gate count for an ECL gate array is really only a figure of merit for the chip.

Although vendors exploit this gate-count confusion in their "one-specmanship" game, they do provide concrete information on how many cells (or fractions of cells) are required to implement a specific logic block in their macro cell library. Therefore, you can count the number of cells required to implement a logic design and use a conservative cell-utilization figure to size the design to a specific array.

Because current ECL gate arrays use a minimum of three metallization layers for global routing, vendors estimate the conservative cell-utilization figure of 70%. Two metal layers are usually reserved for gate interconnections; the third layer is reserved for power and ground. However, AMCC uses all three layers for gate interconnections interspersed with power and ground lines. It specifies an average 95% utilization figure for 100% routing in its Q20000 series. Plessey Semiconductor manufactures the same device and calls it the ELA80K series. Because Motorola's MCA-4 series uses four layers of metal for global routing, it boasts a utilization figure in excess of 80%.

Although multiple layers of metal in large-density ECL arrays assist you in routing gates while using CAD tools, your actual utilization figure may be limited by ECL's old bugaboo—power consumption. Although vendors offer low-and high-power versions of their arrays, virtually all of their packages require heat sinks and air flow to maintain

New Precision Pulse Generator



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maximum junction temperature limits when achieving a high utilization percentage. A low-power package can generally dissipate 15W using a heat sink with air flow. A high-power version might dissipate over 25W, but requires either forced-air convection or liquid-cooling techniques.

Trading speed for power

To conserve power, ECL vendors offer speed-power programming features in their arrays. Speed-power programming allows you to manage the arrays' power consumption by programming the current in the current switches. Each cell has a selection of resistors for the current switches, collector loads, and emitter followers, which let you tailor gates for low-, medium-, or high-power operation (**Fig 2**). To achieve optimal power management, select a speed option when you choose a macro from the cell library.

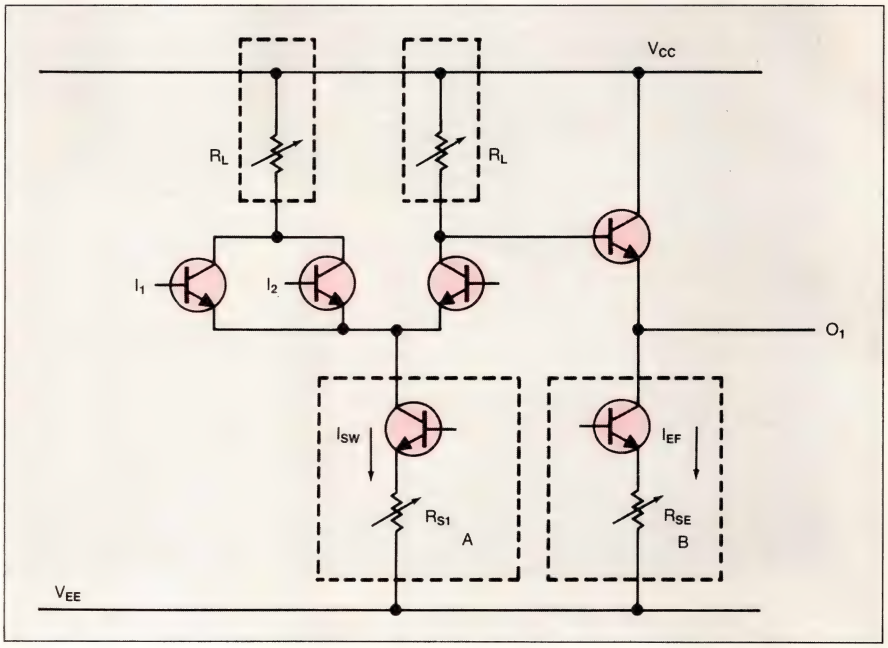


Fig 2—Speed-power programming lets you trade an ECL gate's frequency response for lower power operation. *In this Siemens circuit you can independently program the current switch and the emitter follower for 0.275 mA, 0.55 mA, and 1.1 mA of current.*

Siemens takes speed-power programming one step further by allowing you to mix ECL gates with current-mode-logic (CML) gates. The company's SH100E series, which features gate complexities from 1500 to 16,000 gates, 120-psec gate delays and 1.5-GHz D flip-flop toggle rates, lets you use ECL macros in critical paths, and use the CML macros in slower speed sections, thereby conserving power. A CML gate has the same construction as an ECL gate, but has different bias-voltage generators and no emitter followers.

All of the vendors offer CAD packages that accept data from a schematic-capture program or a simulated netlist generated on a workstation, such as those from Daisy, Mentor, or Valid. The CAD packages let you perform logic simulation (including timing verification), placement and routing, fault simulation, speed-power programming, test-program generation, and back annotation of actual wiring delays for design analysis. Depending on design complexity and the amount of customer involvement, NRE charges from $40,000 to $100,000 to develop a pattern tape for mask generation.

Some dare to be different

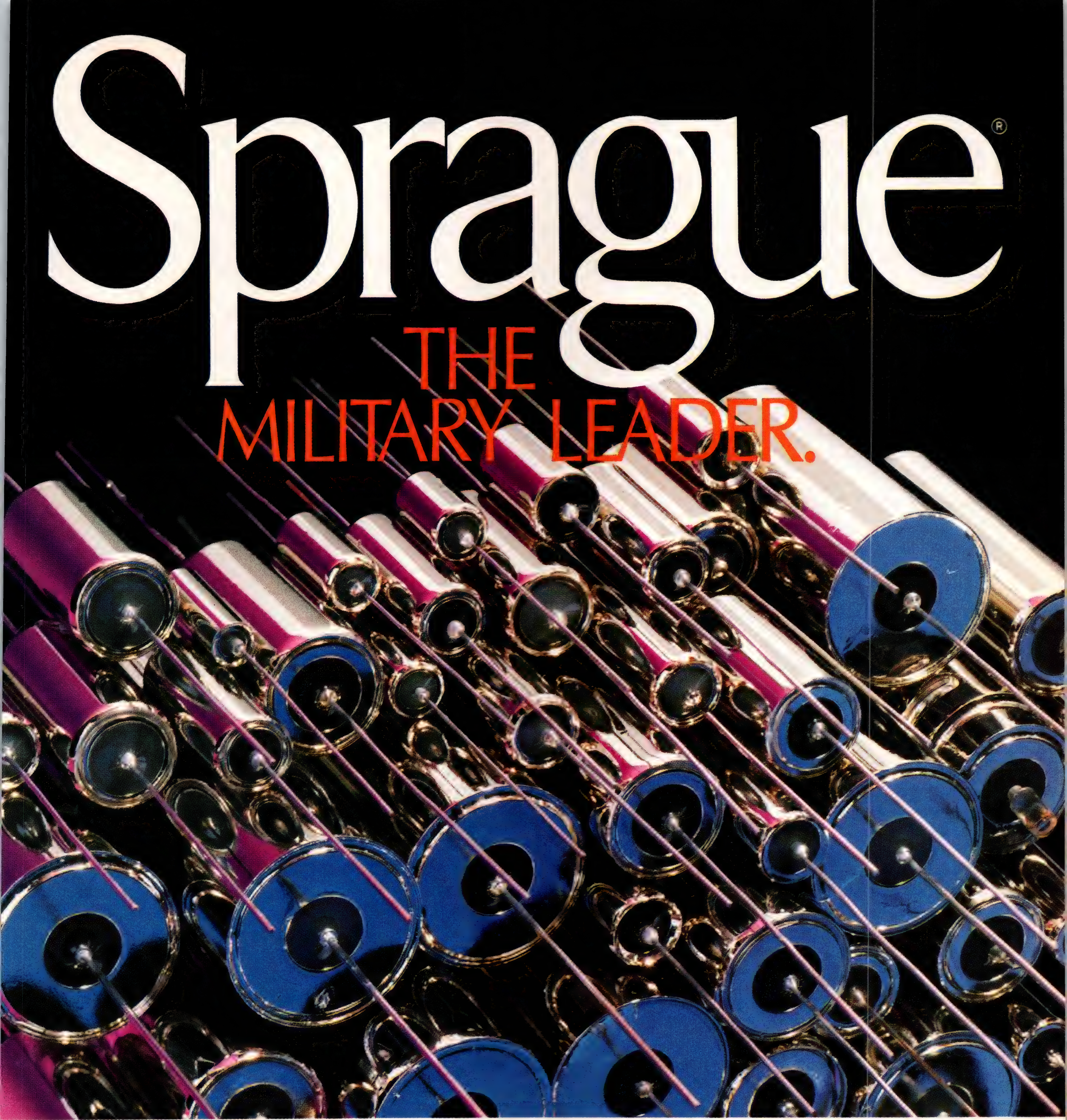
Although ECL gate arrays usually come in a column-by-row arrangement of internal cells surrounded by a periphery of I/O cells, some architectural differences do exist. Raytheon, for example, uses a contiguous-row approach, whereby transistors and resistors are aligned side-by-side in adjacent rows, rather than in grouped cells. The company claims that this arrangement permits a greater number of minimum-addressable programmable sites (MAPS).

MAPS consist of six resistors and six transistors. The bias-voltage generators are located at the ends of the rows. Raytheon's 70E18 and 40E12 arrays also have TTL- and CMOS-compatible I/O interfaces, and their 1ME12 gate array contains a 1.28k-bit RAM cell.

Fujitsu offers a wide assortment of ECL gate arrays with and without RAM cells. The ET2004M, ET2009M, ET3004M, and ET5005M arrays have 4.6k-, 9.2k-, 4.2k-, and 5.1k-bit RAM cells, respectively. They also have 2640, 2640, 3960, and 4928 ECL-equivalent gates, respectively. The devices' interfaces are TTL-compatible, and can be mixed with both 10KH and 100K ECL-compatible interfaces.

Besides offering on-chip RAM cells with 4k- to 180k-bit densities in its MCA-4 gate arrays, Motorola will offer mega functions in the cell library. Examples of these functions include multipliers, barrel shifters, 2-to-5-port register files, and ALU functions. The company claims that the optimized silicon will provide density, speed, and power capabilities rivaling those of full-custom designs.

AMCC products contain a circuit trick that reduces power consump-



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ECL-programmable gate arrays and PLDs

tion and reduces the skew between the rising and falling edges on an ECL output signal. Whereas conventional ECL structures use an emitter follower biased with a current source, the Q20000 series has a propietary discharge circuit (**Fig 3**). The circuit supplements the emitter follower, which provides an active pullup for the load, with a capacitively coupled, pulldown transistor. When the output switches from a high state to a low state, the pulldown circuit provides a turbo discharge for the capacitive load.

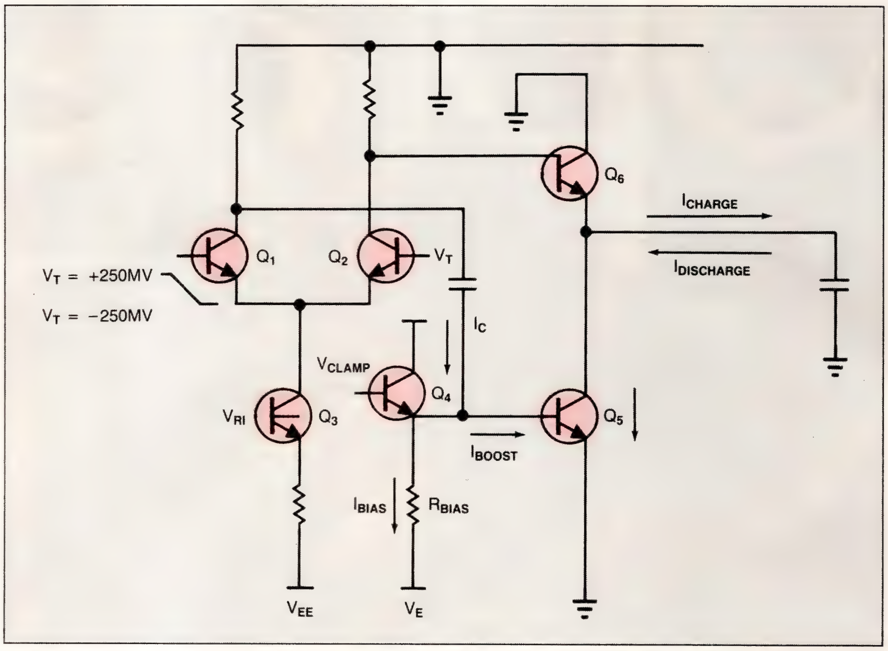


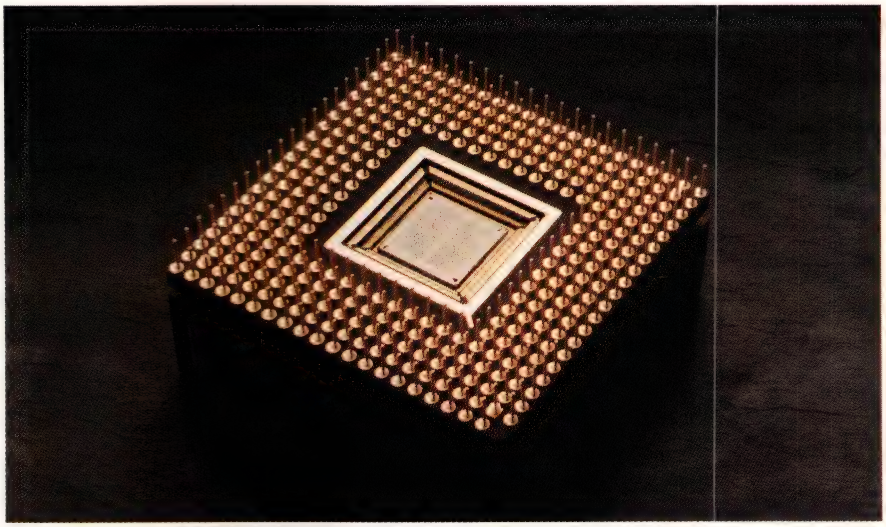
Fig 3—The capacitively coupled pull-down circuit on the output *of the gates in the Q20000 array provides a turbo discharge for capacitive loads. The circuit reduces the overall power consumption and equalizes the skew in the rise and fall times.*

Large arrays have plenty of I/O

Coupled with the high-density arrays, ECL vendors offer a wide range of packages with a large number of I/O ports. All of the arrays claiming to have equivalent-gate

densities greater than 10,000 gates come in versions that have more than 200 I/O ports. Standard packages include pin-grid arrays with pin-fin heat sinks for power dissipation. In addition, Motorola and Siemens offer their arrays on a TAB (Tape Automated Bond) package, which provides as many as 360 leads with pitches as low as 0.004 in.

But, very large density arrays with lots of I/O may not be suitable for your needs. There is no sense in using a gate array with more equivalent gates than is necessary for a particular application. In fact, lower density arrays are often faster than high-density devices because there are fewer gates simultaneously switching and, therefore, less crosstalk in the internal circuitry.

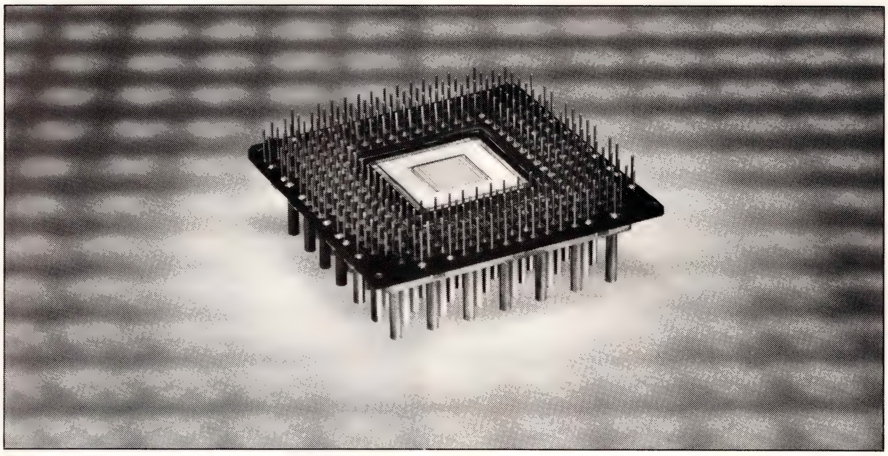


Standard ECL gate-array packages include ceramic pin-grid arrays (CPGA) with pin-fin heat sinks. *Siemen's SH100E array comes in a CPGA with as many as 319 pins.*

Estimating speed, however, requires some caution. The rule of thumb that vendors use when specifying the speed of a gate array is the D flip-flop toggle rate. The toggle rate usually is obtained by connecting the $\overline{Q}$ output directly to the D input on an internal flip-flop. If your circuit requires a gate in the

feedback loop you must factor in the additional gate delay, which lowers the frequency characteristics. In addition, the output buffers often must drive capacitive lines, reducing the overall system speed. You're always better off using the gate-delay figures and metal-propagation delay figures given by the vendor in a worst-case, design-analysis-for-speed estimation.

Even noting this caution, some ECL gate array figures are impressive. Sony's E3G200, a 200-equivalent-gate array, specifies a 2.5-GHz flip-flop toggle frequency; the E3G70, a 70-equivalent-gate array, specifies a 3.5-GHz toggle rate. The family boasts a gate propagation delay less than 100 psec. In addition, Fujitsu's ultra-high-performance series features an array, E128H, which has 128 gates with 75-nsec propagation delays, and a specified D flip-flop toggle rate of 4 GHz.



The tape-automated bonding (TAB) process used in the MCA10000ECL series has 360 leads with inner-lead pitches as small as 0.004 in. *The tape mounts on a 289 PGA with optional pin-fin heatsinks.*

AT&T, which is currently accepting semicustom and custom cell-based design for its BEST-1 series, specifies a 5-GHz D flip-flop toggle frequency, and an 80-psec gate delay for its high-power version, which dissipates 2 mW per gate. The company claims to have fabri-

cated a 5.2G bps MUX and DEMUX, and a 4.6-GHz frequency divider. A design catalog will be available in the fall.

The ECL gate array provides the designer with a variety of tools for complex designs. But experienced designers know that the user-programmable feature of PLDs offers an advantage in designs requiring gate complexities less than 1000. If you commit a system to ECL logic, there are ECL PLDs to "glue" the pieces together. Because you program these devices yourself, using PLD programmers such as those from Advin (Sunnyvale, CA) and Data I/O Corp (Redmond, WA), they can quickly absolve you of any design sins, or implement custom-logic circuitry.

Cypress Semiconductor has two ECL PLD series that use the industry-standard, sum-of-products architecture for PAL devices. The \$20.50 CY10E301 (10KH-compatible) and CY100E301 (100K-compatible) devices have 16 inputs and eight outputs (16P8 configuration). The high-speed versions have maximum input-to-output propagation delays of 3 nsec, and draw a maximum of 240 mA from the supply. The low-speed versions have input-to-output propagation delays of 6 nsec max, and draw 170 mA max.

The \$26.85 CY10E302 and CY100E302 devices have 16 inputs and 4 outputs (16P4 configuration). The high-speed versions feature a 2.5-nsec, input-to-output delay (max), while drawing 220 mA (max); the low-power versions have 6-nsec delays (max) and draw 170 mA (max). All of the products have output-polarity fuses and a security fuse for implementing proprietary logic.

National Semiconductor also offers PLDs in the 16P8 and 16P4 PAL configurations. The company offers two families with maximum input-to-output propagation delays of 6 nsec and 4 nsec, respectively. The PALxx16P8 and the PALxx16P4A (\$19.60 and \$25.60, respectively) are combinatorial devices with either programmable or complimentary 10KH- or 100K-compatible outputs. In addition, the series includes PLDs with registered outputs. Devices with either single-clock or dual-clock inputs are available. The high-speed commercial version specifies a minimum 5-nsec setup time for the registers, a maximum clock-to-output time delay of 3.5 nsec, and a maximum clock frequency of 117 MHz.

ECL-programmable gate arrays and PLDs

For more information . . .

For more information on the ECL gate arrays and PLDs discussed in this article, circle the appropriate numbers on the Information Retrieval Service card, or use EDN's Express Request service. When you contact any of the following manufacturers directly, please let them know you saw their products in EDN.

ECL GATE ARRAYS

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Circle No 700

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Phone (800) 372-2447
Circle No 701

Fujitsu Microelectronics Inc
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Phone (408) 922-9000
FAX 408-432-9030
Circle No 702

Motorola Inc
ASIC Division
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Chandler, AZ 85224
Phone (602) 821-4406
FAX 602-821-4850
Circle No 703

NEC Electronics Inc
401 Ellis St
Box 7241
Mountain View, CA 04039
Phone (415) 965-6381
FAX 415-965-6752
Circle No 704

Plessey Semiconductor
1500 Green Hills Rd
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Phone (408) 438-2900
Circle No 705

Raytheon Co, Semiconductor Div
350 Ellis St
Mountain View, CA 94039
Phone (415) 968-9211
FAX 415-966-7620
Circle No 706

Siemens Inc
2191 Laurelwood Rd
Santa Clara, CA 95054
Phone (408) 980-4566
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Circle No 707

Sony Corp of America
10833 Valley View St
Cypress, CA 90630
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ECL PLDs

Cypress Semiconductor Corp
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Circle No 709

National Semiconductor Corp
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Santa Clara, CA
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FAX 408-245-6340
Circle No 710

The military version of the registered PLD, the $29.95 PALxx16RM4A, specifies a minimum 3-nsec register-setup time, a maximum clock-to-output delay of 2 nsec, and a maximum clock frequency of 200 MHz. All of the PLDs come in 24-pin ceramic DIPs and have security fuses to protect proprietary logic. The company's PLAN software package provides an interactive development tool.

The wide range of speed and density for programmable ECL products makes them attractive for applications in supercomputers, mainframes, military systems, optical data links, and ATE. In addition, their flexibility is enhanced by the fact that BiCMOS and GaAs products operate with 10K-, 10KH-, and 100K-compatible I/O signal levels. This compatibility allows you to mix the logic families without level translators, which operate at lower speeds. EDN

References

1. Gallant, John A, "Gallium arsenide digital ICs complement ECL families in high-speed applications," *EDN*, March 3, 1988, p 79.

2. Tomasetta, Louis R, "Processing advances push GaAs ICs to higher VLSI levels," *EDN*, June 9, 1988, p 243.

Article Interest Quotient
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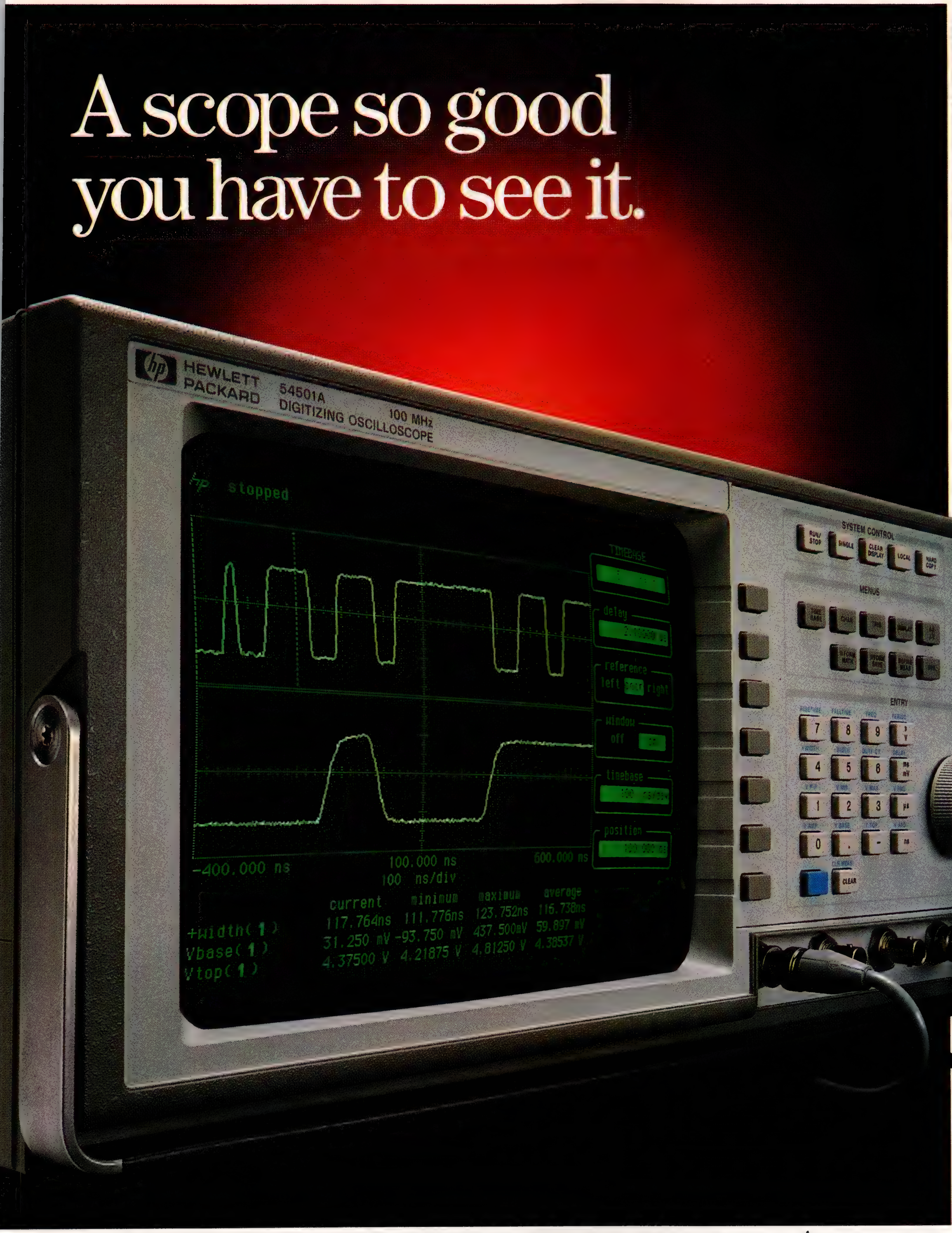
High 518 Medium 519 Low 520

WHAT'S NEXT IN EDN

EDN's September 1 issue will feature a staff-written Special Report on nonvolatile memories, including EPROMs, EEPROMs, flash EEPROMs, and one-time-programmable devices. It will also cover real-time kernels for single-chip microprocessors, ASIC verification testers, and how to keep PC data safe. The next installment of Bob Pease's troubleshooting analog circuits series will also appear in this issue.

In our other September issues, look for reports on signal conditioners and 8- and 16-bit microcontrollers.

You won't want to miss any of these issues.



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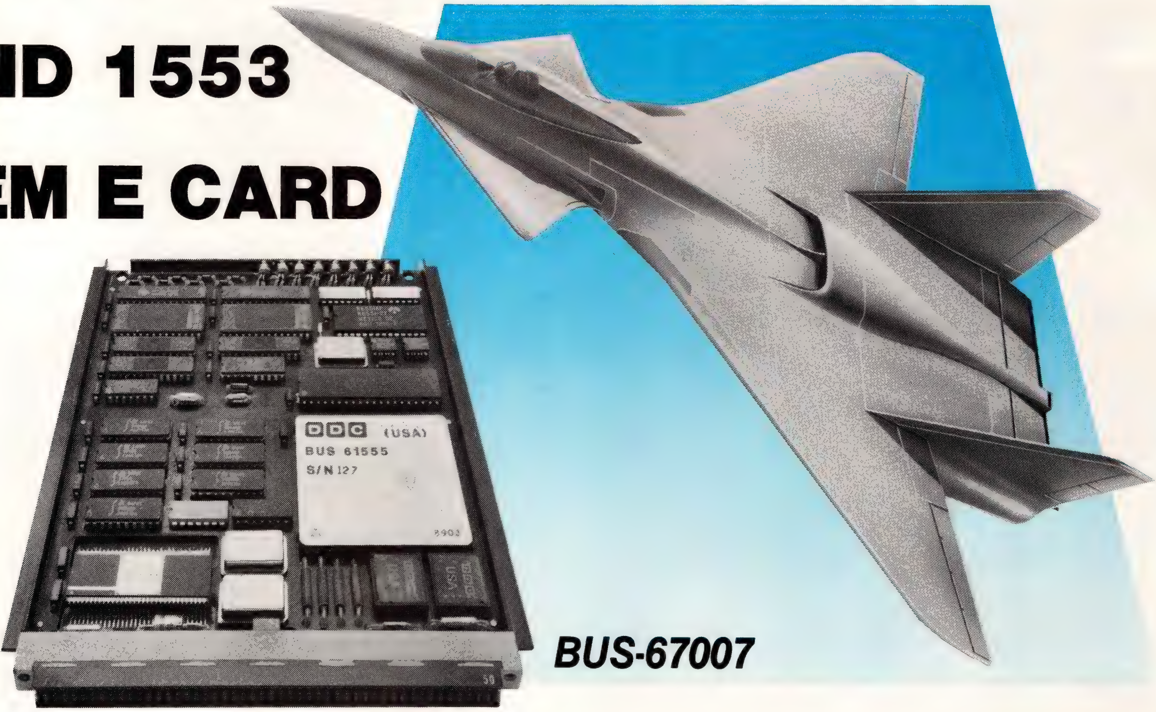
ABOUT SYNCHRO-CONVERSION • A/D & D/A CONVERSION • 1553 BUS DEVICES • POWER & CUSTOM HYBRIDS

1750A MICROPROCESSOR AND 1553 SEM E CARD



DDC's newest Microcomputer SEM E card, the BUS-67007, provides a general purpose, single chip, 16 bit CMOS microprocessor designed for high performance floating point and integer arithmetic, with extensive real time environment support conforming to the MIL-STD-1750A instruction set architecture. The Performance (Pace 1750A) CMOS microprocessor and onboard 32K words of EPROM offers an embedded system controller that can be used as a generic 1750A processor with a BUS-61555, full intelligent dual redundant MIL-STD-1553B Remote Terminal (RTU), Bus Controller (BC), and Monitor (MT). Its RS-422 port facilitates software development and system integration.

The BUS-67007 is packaged on a standard SEM E card with a 150 pin connector. Its on-board 8K x 16 SRAM supports the 1750A CPU. The separate internal 8K x 16 dual access shared RAM of the BUS-61555 AIM-HY supports the 1553B messages, preventing partially updated data from being read by the CPU or transmitted to the 1553 Data Bus. The AIM-HY off-loads the microprocessor from the 1553 communication protocol tasks and offers the host additional RAM for program or data.

Equipped with 8 L.E.D.'s, the card gives visual BIT feedback as to the CPU self-test (green), unrecoverable errors (red), software errors (red), RS-422 status (green), EPROM status (green), SRAM status (green), 1553 terminal self-test status (green), and the CPU watch-dog timer status (green); which can be changed by software for other future meanings. The BUS-67007, requires only 5 volt DC power, with a total power dissipation under 5 watts.

The Microcircuit, Digital, CMOS, 16-BIT MIL-STD-1750A MICROPROCESSOR, is on DESC drawing #5962-87665-01XC. The PACE 1750A CPU are also available in CMOS/SOS technology for radiation environment applications, in production by 1990. DDC's AIM-HY, BUS-61555 Terminal is on DESC drawing #5962-88692-01XC. The BI-POLAR & CMOS-SOS technology used is available to support tactical and strategic environments.

For additional information on the BUS-67007, contact Steve Friedman at toll-free 1-800-DDC-1772 (outside New York) or call the DDC office nearest you. □

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It also lets you easily check your equations with a 12-character alphanumeric display that can scroll through up to 80 characters for long equations. And, the last equation replay feature lets you edit or check the last computation without having to go back and reenter it.

In addition, when you need to solve quadratic, cubic or quartic equations, the TI-68's polynomial root finder will calculate the real and complex roots — automatically.

Working with number bases and conversions are also no problem. Perform arithmetic functions in decimal, hexadecimal, octal or binary. And it does Boolean logic operations, too.

The TI-68 provides up to 440 program steps for as many as 12 user-generated formulas. It even stores up to 36 values in memories with user-defined alphanumeric names.

The TI-68 has what you've been looking for — the right functionality at the right price. See and try it at a nearby retailer, or call 1-806-747-1882 for additional information and to request free product literature.

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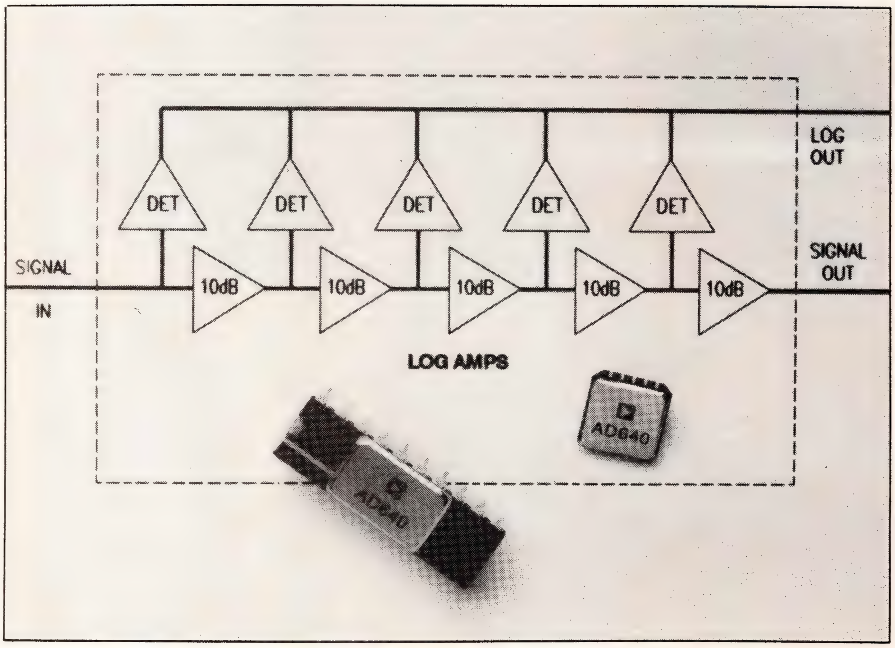
CIRCLE NO 60

Log amp features 50 dB of dynamic range for input frequencies from dc to 120 MHz



The AD640 log amp integrates five detector stages *to provide 50 dB of dynamic range, and is fully calibrated for stable performance over its entire temperature range.*

The AD640 dc-coupled logarithmic amplifier is a monolithic, completely analog device that features a dynamic range of 50 dB, a maximum dc nonlinearity of ±0.6 dB, and a 120-MHz bandwidth. Log amps are useful in such instrumentation applications as spectrum and network analyzers, and they can compress wideband data prior to A/D conversion, thereby reducing the A/D converter's dynamic-range requirements.

The log amp uses a successive-detection scheme to provide an output current proportional to the input voltage's logarithm. You can convert the differential-output current to a voltage by using the device's internal resistors and a high-speed op amp.

The log amp is unique because it integrates five cascaded, dc-coupled, amplifier-limiter stages in one IC. Each stage has an associated full-wave detector whose output current depends on the absolute value of its input voltage. The five outputs are summed to provide the video output, which is scaled at 1 mA per decade or 50 μA per dB. The bandwidth of each stage has a small-signal voltage gain of 10 dB and a −3-dB bandwidth of 350 MHz. The bandwidth of all five stages together is guaranteed at 120 MHz.

Two key performance features of the log amp are its full calibration and its temperature performance. The device's logarithmic response is absolutely calibrated to within ±1 dB for dc or square-wave inputs from ±0.75 mV to ±200 mV; the scaling is also guaranteed for sinusoidal inputs. An internal X10 attenuator provides an alternative input range of ±7.5 mV to ±2V dc. The intercept voltage (the input voltage for which the log amp's output is zero) is calibrated to exactly 1 mV. The log amp's internal architecture minimizes thermally induced errors so that the logarithmic slope, intercept voltage, and ac response are stable over the full military temperature range.

You can cascade two log amps by simply tying the balanced signal output from the first amp to the input pins of the second amp. However, because of noise coupling between the two amps, cascaded configurations require a tradeoff between bandwidth and dynamic range. You can achieve a higher dynamic range of 95 dB at a reduced bandwidth of 10 Hz to 100 kHz by including a low-pass filter between the two devices. For bandwidths of 50 to 150 MHz, the two cascaded converters can achieve a dynamic range of 70 dB.

The log amp operates from ±4.5 to ±9V supplies (±5V typ), and consumes a maximum of 375 mW. The device is available in industrial (−40 to +85°C) and military (−55 to +125°C) temperature ranges. Both devices are available in either 20-pin LCCs or ceramic DIPs. The industrial ceramic-DIP version costs $60 (100).

—Anne Watson Swager

Analog Devices, Box 9106, Norwood, MA 02062. Phone (617) 329-4700.

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MODEL	CONFIG-URATION	SPEED (ns)	PACKAGE
CXK5863P CXK5863M CXK5863J	8K x 8 8K x 8 8K x 8	25/30/35 25/30/35 25/30/35	DIP 300 mil SOP 450 mil SOJ 300 mil
CXK5464AP CXK5464AJ	16K x 4 16K x 4	25/30/35 25/30/35	DIP 300 mil SOJ 300 mil
CXK5465P* CXK5465J*	16K x 4 16K x 4	25/30/35 25/30/35	DIP 300 mil SOJ 300 mil
CXK5164P CXK5164J	64K x 1 64K x 1	25/30/35 25/30/35	DIP 300 mil SOJ 300 mil
CXK5971P CXK5971J	8K x 9 8K x 9	25/30/35 25/30/35	DIP 300 mil SOJ 300 mil
CXK58258AP CXK58258AJ	32K x 8 32K x 8	25/30 25/30	DIP 300 mil SOJ 300 mil
CXK58258P CXK58258SP	32K x 8 32K x 8	35/45 35/45	DIP 600 mil DIP 300 mil
CXK54256P	64K x 4	35/45/55	DIP 300 mil
CXK51256P	256K x 1	35/45/55	DIP 300 mil
*O/E			

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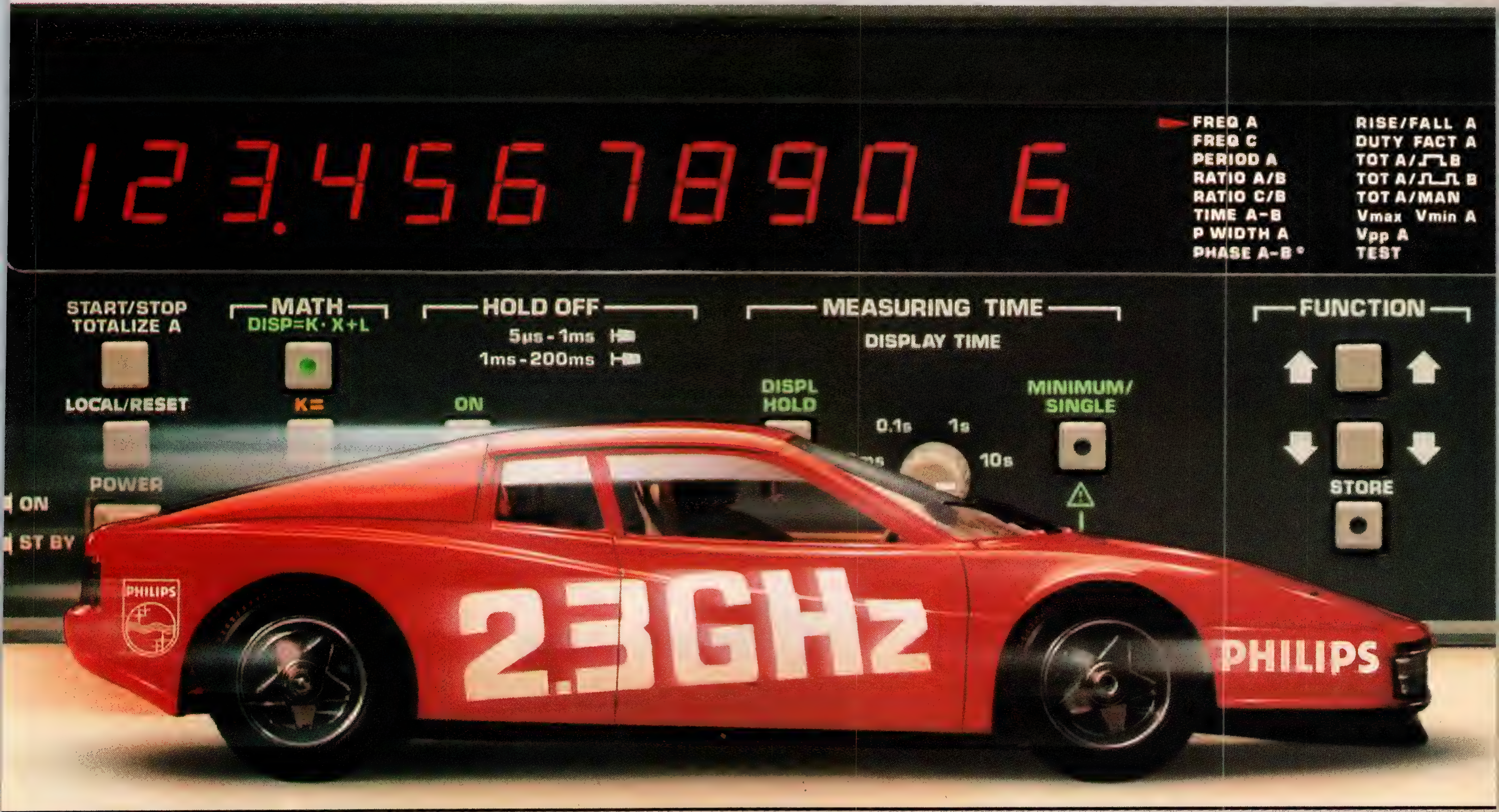

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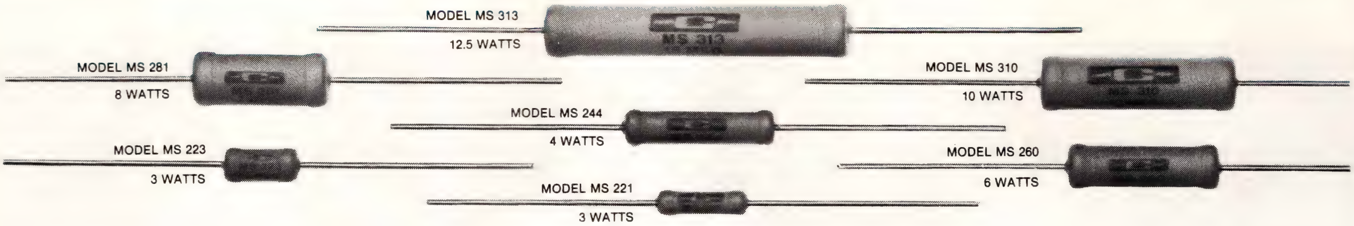
ADVANCED TECHNOLOGY MADE TO MEASURE

PHILIPS

Type MS Non-Inductive Power Film Resistors from CADDOCK optimize high-speed power switching:



1. Caddock's "Non-Inductive Design" can improve rise and fall times to minimize losses in power switching circuits.

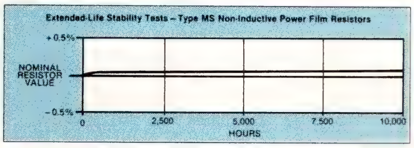
To keep the inductance to an absolute minimum, the special serpentine pattern provides for neighboring lines to carry the current in opposite directions to achieve maximum cancellation of flux fields over the entire length of the resistor.

The result is a truly non-inductive resistor that is about as inductive as a straight piece of wire the length of the resistor body.

This makes it possible for engineers to design new circuit configurations with superior non-inductive performance.

2. Extended-life stability that is typically better than 0.05% per 1000 hours.

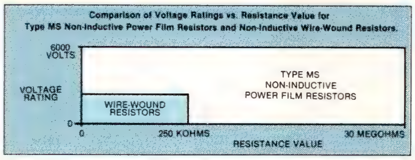
Extended load-life tests at full power have demonstrated typical stability better than 0.05% per 1000 hours.



Detailed stability data is included in the "Reliability Test Summary – Caddock Report #1" which is available on request.

3. Critical resistance values extended by higher voltage and power ratings.

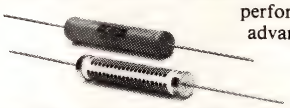
Caddock's Micronox® film resistor technology permits single-resistor voltage ratings as high as 6000 volts to be combined with power ratings of 12.5 watts at +25°C. This combination of power and voltage provides a critical resistance value of 2.88 Megohms - more than 10 times higher than can be achieved with wire-wound construction.



The higher voltage rating of Type MS resistors also overcomes the resistance value limits imposed on wire-wounds by the minimum wire size and spacing.

4. The special construction of Micronox® resistors assures high performance through harsh environments.

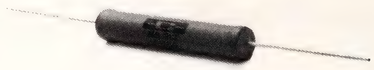
Type MS Power Film Resistors are produced by firing high-stability Micronox® resistance films directly onto a solid ceramic core - in air - at +1400°F to achieve a structure with these special performance advantages:



- Operating temperatures as high as +275°C.
- Repeatable temperature characteristics that include a TC of only 50 PPM/°C.
- Verified reliability through environmental extremes encountered in both 'down-hole' oil exploration and deep-space instrumentation equipment.

5. The family of Type MS Power Film Resistors includes 14 models with single-resistor values to 30 Megohms.

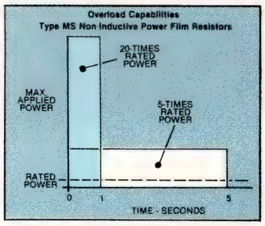
To overcome the construction *and* cost limitations inherent in wire-wound resistors, Caddock Micronox® film resistor technology gives circuit designers a *practical* balance between performance, value, size and cost, as the specifications for the Model MS 313 demonstrate:



- Non-inductive performance.
- 12.5 watt power rating.
- Resistance values from 50 ohms to 30 Megohms.
- Resistance tolerances from ±1.0% to ±0.1%.
- Maximum operating voltage of 6000 volts.
- Unit prices below $2.50 on 1000-lot orders for any value between 100 ohms and 200 Kohms.

6. Overloads of 5-times rated power for 5 seconds and 20-times rated power momentary are standard on all models.

After repeated power overload tests that apply 5-times rated power for 5 seconds, Type MS resistors have demonstrated stability typically better than 0.1%



For even higher overload situations, Type MS resistors can be subjected to 20-times the rated power for one second.

Caddock's advanced film resistor technology is the source of these outstanding advantages – advantages that are matched by a 25-year record of outstanding 'in-circuit' reliability.

Discover how easily these problem-solving resistors can improve the performance and reliability of your equipment, too. For your copy of the latest edition of the Caddock 28 page General Catalog, and specific technical data on any of the more than 200 models of the 19 standard types of Caddock High Performance Film Resistors, just call or write to –

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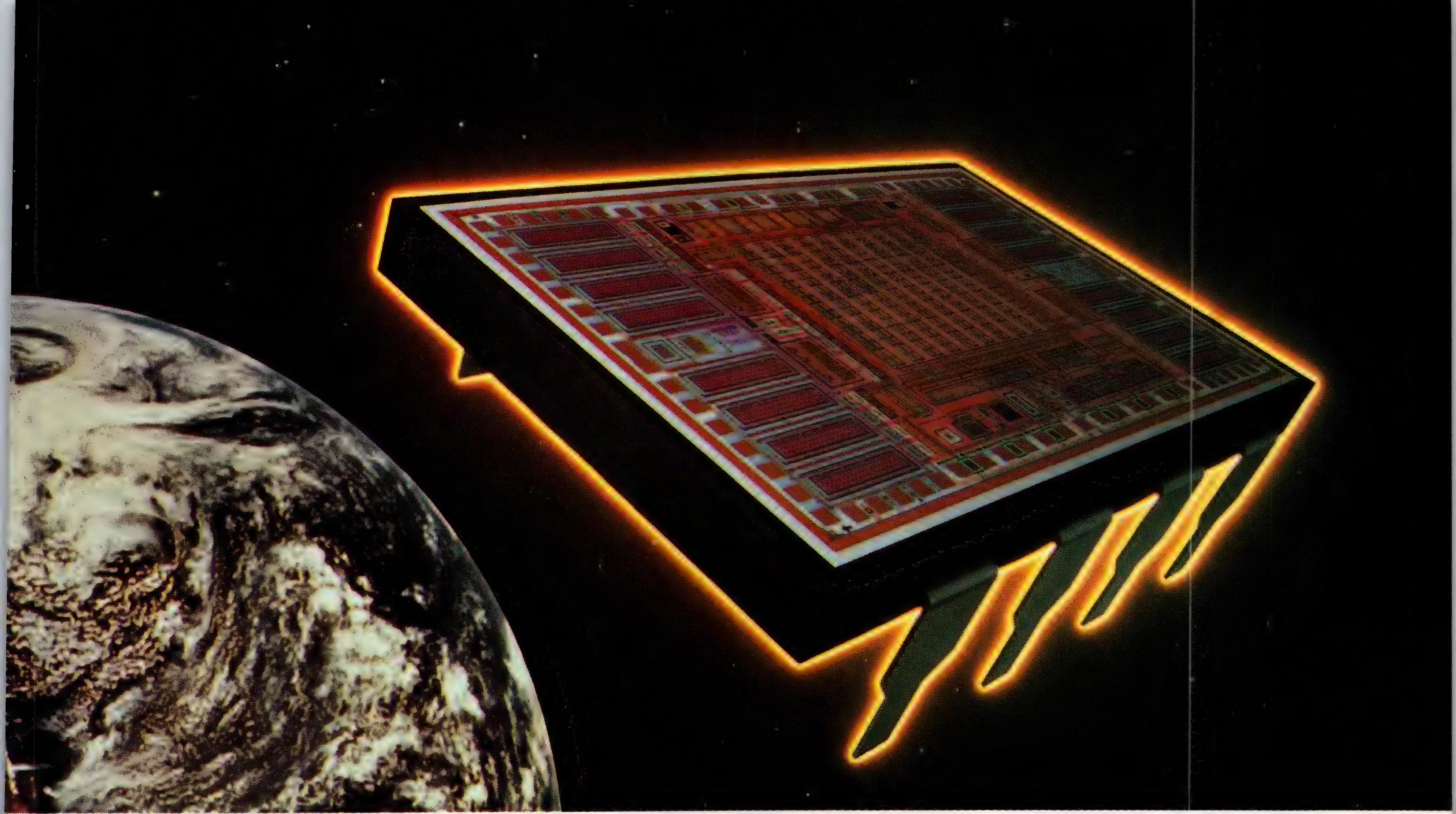


REAL-TIME

EDN SPECIAL REPORT

Ada supports the enormous, complex programs that are vital to real-time military systems. (Photo courtesy Alsys Inc)

Ada

MILITARY TECHNOLOGY

The growing use of 32-bit μPs, with their 4G-byte address spaces, allows engineers to create embedded systems incorporating truly gargantuan programs. Popular programming languages are hard pressed to support programs forged with megalines of code, but Ada meets that challenge.

***Steven H Leibson**, Regional Editor*

"Please put down your weapon. You have 20 seconds to comply," stated the ED-209 law-enforcement droid.

The intimidated junior executive dropped his chrome-plated pistol like a hot potato. This boardroom demonstration had gone far enough. Unfortunately, the junior exec's conciliatory action went unnoticed by the ED-209.

"You now have 15 seconds to comply," it said. The droid proceeded to count down the seconds as the other executives scurried out of the way. Meanwhile, a host of technicians tried to shut down the ED-209.

"I am now authorized to use force," said the droid, as it blasted the unfortunate junior executive into oblivion with its automated weapons.

The corporate CEO looked up at his senior VP, the man responsible for the ED-209 project, and said "Dick, I'm very disappointed."

"I'm sure it's only a glitch," replied the senior VP.

This scene from Orion Pictures' 1987 movie *Robocop* may seem fantastic, but it illustrates the very real problems engineers face today as they give real-time embedded systems expanding physical abilities and ease humans out of the control loop. We already entrust machines far more dangerous than the ED-209 to embedded-computer control. Computers now run such items as mechanical and chemical manufacturing plants and nuclear-tipped cruise missiles. As embedded-control computers continue to find their way into complex military systems and commercial products, the enhanced functions of these systems press engineers and programmers to create increasingly complex software. Although computers can serve as very reliable overseers, a programming error in a real-time embedded system can have costly, or even fatal, consequences. The Ada programming language was created with these issues in mind.

***Ada and a personal computer** from Zenith operate this UH-60A Black Hawk helicopter trainer for the army. The Ada development system is from Alsys. Many flight simulators and trainers, excellent examples of real-time applications, now incorporate Ada code. (Courtesy Validity Corp)*

In the 1970s, the DoD started to take a serious look at its software-procurement policies.

The US Department of Defense (DoD) has a keen interest in using computers to control physical processes in air, land, sea, and space vehicles, as well as in weapons systems. Hence, the DoD has been doubly concerned about the safety, reliability, maintainability, and cost of the software that runs such systems, and decided in the 1970s to seriously examine its software-procurement policies. The DoD's software study in 1974 showed a reversal of the ratio of hardware to software procurements from the 1950s to the 1980s. In the 1950s, 80% of the DoD's acquisition budget for new systems was used for hardware, and the DoD projected that software would consume that percentage in the 1980s. That projection was correct; by 1990, the DoD will be spending more than $10 billion a year on software.

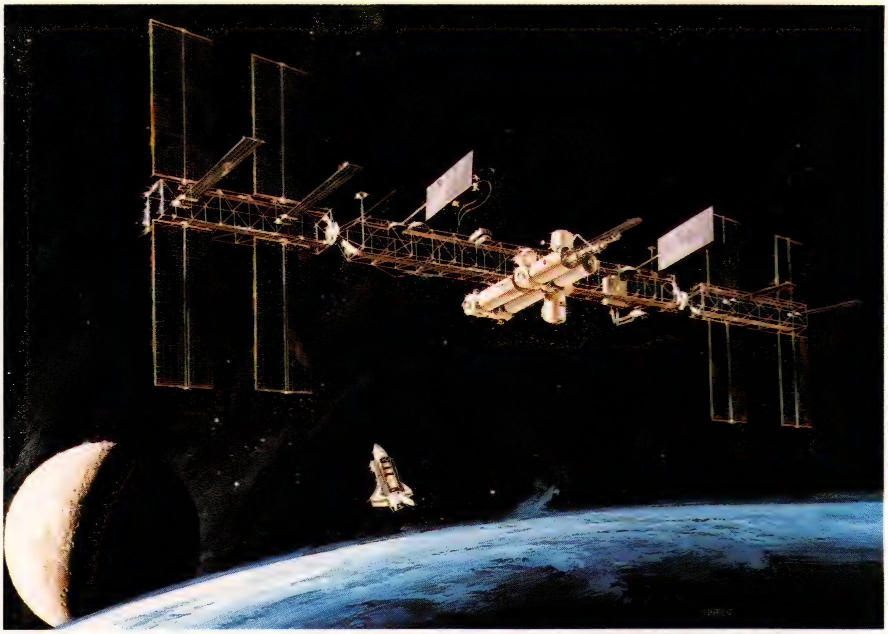
The 1974 study also revealed that DoD contractors were using several hundred programming languages and dialects to create defense systems. This multitude of diverse languages was causing support costs to skyrocket. Some of these languages were so esoteric that only a few programmers were skilled in them, guaranteeing maintenance problems in years to come. When a deployed system can no longer be supported, it must either be totally redesigned or scrapped.

The software monster grows exponentially

Software program size has grown exponentially over time with each new deployed system (**Fig 1**) as more powerful military computers have become available. In addition to jet fuel, the B2 bomber will fly on an estimated 2M lines of code (LOC). The software programs for both the ATA and ATF advanced military aircraft projects will run an estimated 10M LOC each. NASA has adopted Ada as the official programming language of the Space Station Freedom Project, and expects the computerized systems aboard the space station—as well as the associated ground-support sys-

TABLE 1—REPRESENTATIVE ADA DEVELOPMENT SYSTEMS FOR EMBEDDED REAL-TIME APPLICATIONS

VENDOR	COMPILER	HOST CPU	TARGET PROCESSOR	PRICE
AITECH	AI-ADA/020	DEC VAX/VMS	68020	$12,500–$79,875
	AI-ADA/88K	DEC VAX/VMS	88000	$40,000–$80,000
ALSYS	C11rX68	DEC VAX/VMS	68000/10/20/30	$35,000 FOR VAX 62XX, 8300, 8350, AND 8530. PRICES VARY FOR OTHER VAX MODELS.
	P07-C12-X68	HP9000/300	68000/10/20/30	$20,000
	P07-C15-X68	SUN 3	68000/10/20/30	$20,000
	P07-C19-X86	IBM PC (286 OR 386)	8086/186/286	$20,000
	P07-C28-X68	IBM PC (286 OR 386)	68000/10/20/30	$20,000
	P07-C36-X68	APOLLO WORKSTATIONS	68000/10/20/30	$20,000
DDC-1	DACSr80 x 86	DEC VAX/VMS	8086/186/286/386	$30,000–$90,000
INTEL	VVSADA386	DEC VAX/VMS	80386	$24,000–$86,000
	VVSADA960	DEC VAX/VMS	80960	$28,000–$90,000
INTERACT	1750A CROSS-COMPILER SYSTEM	DEC VAX/VMS	1750A	$8000–$100,000
NATIONAL	NSW-ADA-BRVM	DEC VAX/VMS	32000 FAMILY	$43,500–$88,000
RATIONAL	1750A CROSS-DEVELOPMENT FACILITY	RATIONAL R1000	1750A	$31,850–$78,400
	68000 CROSS-DEVELOPMENT FACILITY	RATIONAL R1000	68000/10/20	$31,850-78,400
READY SYSTEMS	RTADA/SUN TO 68020	SUN 3	68020	$19,500
	RTADA/VMS TO 1750A	DEC VAX/VMS	1750A	$22,500–$98,000
	RTADA/VMS TO 68020	DEC VAX/VMS	68020	$19,500–$89,000
SOFTECH	ADA-86	DEC VAX/VMS	8086/186/286/386	
TARTAN LABS	VMS 1750A	DEC VAX/VMS	1750A	$15,000–$90,000
	VMS 68K	DEC VAX/VMS	68000/10/20	$15,000–$90,000
TELESOFT	TG2027X	DEC VAX/VMS	68000/10/20	$15,000–$80,000
	TG2031X	DEC VAX/VMS	1750A	$15,000–$86,000
VERDIX	VADS	DEC VAX/VMS	1750A	$15,000–$70,000
	VADS	SUN 3, DEC VAX	68020/030	$15,000–$70,000
	VADS	DEC VAX/VMS	80386	$20,000–$75,000



NASA's Space Station Freedom Project employs Ada *as the primary programming language for all mission software in flight hardware and for ground support. The space station will incorporate 10 distributed-computer networks to operate the onboard systems.*

tems—to require several million LOC. These larger programs take much longer to write, and this situation often leads to slipped schedules and ruined budgets. In addition, imperfect coupling between blocks of code written by different programmers or programming groups often causes large programs to be infested with bugs.

Because exponential program growth, plagues of program bugs, cost overruns, and missed deadlines were ominous trends, the DoD formed the High Order Language Working Group in 1975 to determine whether a single programming language could meet all of the DoD's software needs. After years of effort, the result of that work is the Ada programming language, MIL-STD-1815A. The DoD trademarked the name "Ada" so it could maintain control over the language. To be legally called an Ada compiler, a compiler must pass a suite of more than 3000 validation tests and be revalidated annually. The DoD doesn't validate supersets or subsets of the language.

Ada is a complex programming language that was designed for writing very large programs, so most Ada compilers generate code for 32-bit processors. A few 16-bit μPs are also supported. In addition, most Ada development systems run on minicomputers (the Digital Equipment Corp's VAX series is generally preferred), and a few run on engineering workstations and high-end PCs. **Table 1** lists several Ada development systems for real-time applications.

Although initially created for defense systems, Ada's features are designed to solve problems encountered by both commercial and military software projects. Even though both military and civilian project planners are concerned about correct and reliable code that can be easily maintained, Ada was used first for defense systems, because of the so-called Taft directives. Cre-

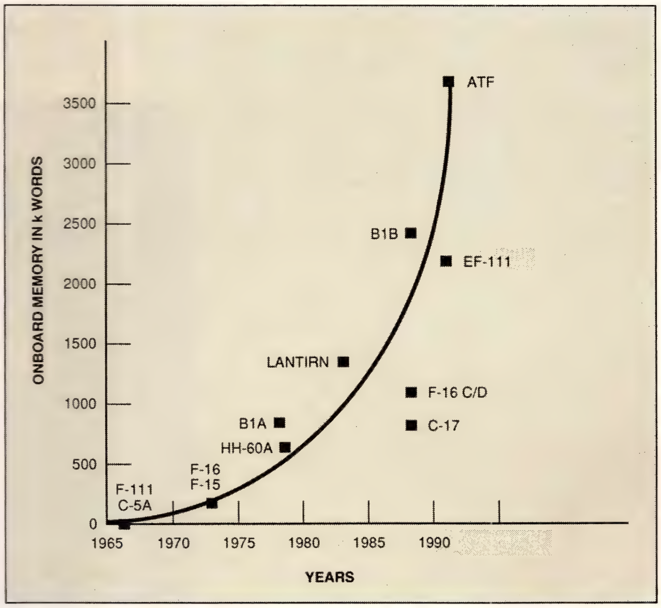


Fig 1—Program size in deployed defense systems *has risen exponentially over time since the introduction of military computers.*

Ada's features are designed to solve problems encountered by both commercial and military software projects.

ated in 1984, the Taft directives require all new software and major software upgrades for mission-critical systems to be written in Ada. In previous years, the DoD issued many waivers to the Taft directives, but the growing number of validated Ada compilers and improving Ada compiler technology will make those waivers harder to get.

Meanwhile, success stories about Ada are starting to appear, primarily in military systems (thanks to the Taft directives). Ada has been used successfully for aircraft trainers, such as the UH-60A Black Hawk Composite Trainer built by Validity Corp (Encinitas, CA), and for missile guidance systems, such as the improved Hellfire missile developed by Rockwell International's Missile Systems Division (Duluth, GA). These two applications have stringent real-time requirements.

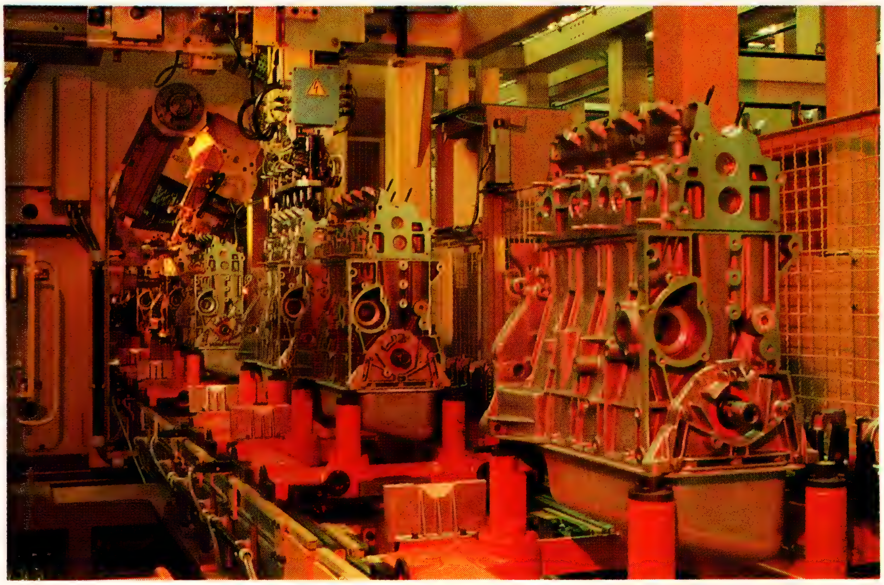
Commercial companies are also starting to use Ada in operational systems. Volvo in Sweden and Citroën in France use Ada for robotic assembly of automobiles. Several telecommunications companies are gearing up to use Ada for central-office switching applications. Appropriately enough, considering its focus on large programming projects, Ada is being used for the world's largest computer system—the global telephone network.

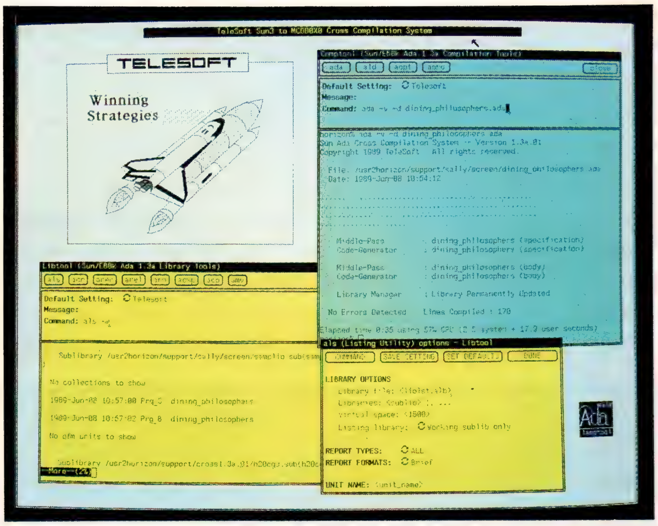
NASA selected Ada as the primary programming language for the Space Station Freedom Project because the space station's software programs will be of staggering size, even by the limits now set by military systems. When it flies in the mid 1990s, the space station will incorporate 10 computerized control systems built from distributed μP networks. These computerized control systems will operate the facility's propulsion; guidance and navigation; electrical power; thermal- and fluid-management; operations- and data-management; and communications and tracking systems.

Despite these successes, the earliest attempts to use Ada for real-time applications failed because the compilers were immature, and because nobody knew how to employ the language to create real-time systems. These early failures make great horror stories; you've probably heard or read many negative opinions about the language (in addition to some of the propaganda disseminated by Ada boosters). To evaluate Ada objectively as a development tool for your next real-time project, you must first shed the myths that have grown around the language.

MYTH: Ada was designed by committee and looks like a camel that was supposed to be a horse. In reality, Ada was not designed by committee. Dr David Fisher at the Institute for Defense Analyses created a draft requirement called Strawman that defined a universal programming language for the DoD's software needs. Based on comments from both military and civilian advisors, this draft went through two revisions, dubbed Woodenman and Tinman. No existing programming language met all of the requirements of the Tinman specification, so in 1977 the DoD produced another revision called Ironman, and contracted four vendors to develop preliminary languages based on

__Ada helps build automobiles__ at a Citroën plant in France. An Ada development system from Alsys helps the auto manufacturer create simulators for robotic assembly equipment.





Certain Ada development systems run on workstations *instead of minicomputers. This Telegen2 cross-development system from TeleSoft operates in the windowed environment of a Sun 3 workstation from Sun Microsystems.*

this refined set of requirements.

The resulting four languages were color coded (blue, green, red, and yellow) to disguise the developers. The DoD then distributed the four languages to interested parties for review. Two of the languages (red and green) survived this review, and their respective developers (Intermetrics of Cambridge, MA and Cii-Honeywell Bull of France) worked to refine their languages against a final specification called Steelman. The refined versions of the two languages competed, again through review, and the DoD selected the language from Cii-Honeywell Bull as the final version of Ada. Thus Ada evolved through competitive design; it wasn't patched together by a committee of pie-in-the-sky academics. The final design decisions were made by either Dr Jean Ichbiah (who later founded Ada-compiler vendor Alsys) or his hand-picked assistants.

MYTH: Ada is too big to learn and too unwieldy to use. The entire Ada language encompasses only 63 reserved words (**Table 2**)—a fairly small number compared with a more widespread and less-feared language such as Microsoft Basic, which comprises some 200 commands, statements, and functions. Ada's power is derived from its flexible use of these few key words. Although 63 reserved words may not qualify Ada as a reduced-instruction-set, high-level language, this small number of words undermines the myth that Ada is too big to learn.

Conversely, Ada provides tremendous flexibility for using these reserved words, so proficient use of the language does require a fair amount of study. Also, Ada incorporates a few unfamiliar concepts, such as tasking and separately compiled program units, that require you to make certain mental adjustments.

The compilers must accommodate every Ada feature, but few programmers use every facet of any programming language. Therefore, you don't have to learn all of Ada's nuances before you can begin using it. In this sense, Ada is no more difficult to use than other programming languages. As with any development tool, if you want to use the novel features of the language, you'll have to study them. Many programmers have already used Ada successfully to produce very large and complex systems.

MYTH: Ada is too slow to use for real-time applications. This myth has a factual basis; early Ada compilers were indeed too slow for many real-time requirements. However, "too slow" is a relative term, because some electromechanical systems define system speeds in tens or hundreds of milliseconds, and other systems require microsecond response times. At a certain point, any programming language becomes too slow to meet the application requirements. Most Ada users acknowledge that the performance problems that once existed have largely disappeared over the last two years, as the compilers have matured. Improved optimization schemes (see **box**, "Compilers optimize Ada for speed"), faster runtime executives, and alternative interrupt mechanisms have been key factors in boosting Ada's real-time performance.

MYTH: Ada stunts a programmer's creativity be-

TABLE 2—ADA's RESERVED WORDS

ABORT	EXCEPTION	PRIVATE
ABS	EXIT	PROCURE
ACCEPT	FOR	RAISE
ACCESS	FUNCTION	RANGE
ALL	GENERIC	RECORD
AND	GOTO	REM
ARRAY	IF	RENAMES
AT	IN	RETURN
BEGIN	IS	REVERSE
BODY	LIMITED	SELECT
CASE	LOOP	SEPARATE
CONSTANT	MOD	SUBTYPE
DECLARE	NEW	TASK
DELAY	NOT	TERMINATE
DELTA	NULL	THEN
DIGITS	OF	TYPE
DO	OR	USE
ELSE	OTHERS	WHEN
ELSIF	OUT	WHILE
END	PACKAGE	WITH
ENTRY	PRAGMA	XOR

To objectively evaluate Ada as a development tool for your next real-time project, you must first shed some myths that have grown around the language.

cause it enforces a rigid programming style. This notion is true only if sloppy work, sneaky programming tricks, and incomplete documentation pass for creativity. Ada enforces software engineering concepts such as code and data abstraction, documentation, and modularity. These characteristics are absolutely required for large programming projects that span several months or years and involve many programmers. When people leave their jobs, others can continue the work easily if the programs are written using a structured tool such as Ada.

Taking the longer view, a well-constructed (engineered) program makes it easier and more economical to maintain software over a long product life (a prime concern of the DoD), and it allows a programmer to make program improvements and additions years after the original author has gone. Archaic programming styles make software maintenance and enhancement impossible. Nevertheless, many companies perpetuate the use of software that is decades old, simply because no one knows how the programs work anymore, and no programmer dares to touch the golden code in case

Compilers optimize Ada for speed

Compilers must generate fast code if Ada is to be a viable language for real-time embedded systems. Optimizations can make or break a compiler's suitability for such applications. Although compilers can create very inefficient assembly-language code, the compiler's optimizer relentlessly applies a large number of optimization techniques that can tremendously reduce the inefficient assembly language generated by the compiler. Consequently, compiler vendors are applying a long list of optimization techniques to the problem of speeding up and slimming down programs written in Ada. Several of these techniques are listed in **Table A.**

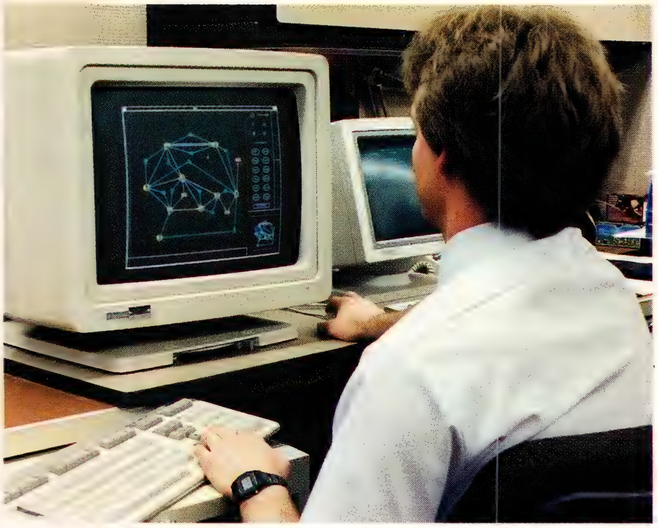
TABLE A—COMPILER OPTIMIZATION TECHNIQUES

- IN-LINE CODING OF SUBROUTINE CALLS
- REGISTER UTILIZATION
  - GRAPH COLORING
  - BASE REGISTER ALLOCATION
- PEEPHOLE OPTIMIZATION
- STACK ALLOCATION
- CONSTANT EVALUATION
- LOOP OPTIMIZATION
  - LOOP INVARIANTS
  - LOOP INTERCHANGE
  - LOOP FUSION
  - LOOP EXPANSION
- CONSTRAINT ELIMINATION
- COMPILE-TIME EVALUATION OF CONSTRANTS
- ALGEBRAIC SIMPLIFICATION
- EXPRESSION ORDER
- BRANCH ELIMINATION
- DEAD CODE ELIMINATION
- LIBRARY OPTIMIZATION
- DEAD VARIABLE ELIMINATION
- INTER-UNIT OPTIMIZATION
- GENERIC SHARING
- CONSTANT PROPAGATION
- LITERAL POOLING
- STRENGTH REDUCTION
- COMMON SUBEXPRESSION ELIMINATION
- TEST MERGING
- BOOLEAN EXPRESSION
  - OPTIMIZATION
  - DEMORGANS
  - PACKING
- STATIC ELABORATION

Because Ada's programming style emphasizes modularity, Ada programs tend to incorporate many subprograms and subroutines. However, in-line code runs faster than code that calls subroutines. Subroutines called only once can be safely placed in line. This step eliminates subroutine-call overhead and return-adedress storage, and it reduces both program storage space and program execution time. A compiler may automatically generate in-line subroutine calls, or you may invoke in-line code through Ada's "inline" pragma. If the subroutine is used several times within the program, the insertion of in-line code may increase storage requirements, but the program will still run faster.

Careful use of CPU registers also allows a program to run faster. Registers provide faster access to program variables than do RAM locations. A technique called graph coloring lets an optimizer evaluate variable usage

a programming error causes an accident. Ada alone can't change this unfortunate situation, but the language's structure helps you create an environment for engineered program development.



Graphic development tools for Ada programs, such as this directed-graph editor and code generator developed by the Westinghouse Electronic Systems Group (Baltimore, MD), drastically reduce the apparent complexity of an embedded design and clarify the various subunits within a program.

Ada promotes software engineering over hacking

Ada is a structured programming language, which primarily means that programs written in Ada make liberal use of "begin" and "end" statements. Structured programming isn't new, but it is a cornerstone of software engineering. Moreover, Ada's features also sup-

and assign the most frequently used variables to registers. Similarly, peephole optimization eliminates superfluous loads, stores, and comparisons when the desired information is already available in a register. Often, peephole optimizers recognize common code sequences that are frequently generated by the compiler and replace these sequences with prepared code sequences that have been specially engineered to run faster.

Loop optimizations also speed program execution by moving as much code as possible out of the loop. Although you should always strive to keep as much code out of a loop as possible, an optimizer may compress even lean loops by pushing some of the assembly language emitted by the compiler's code generator outside of the loop. Short loops can be unrolled into in-line code to save execution time at the expense of code size. You can invoke such an optimization by using Ada's "optimize (Time)" pragma.

Ada programs spend a lot of time performing constraint checks; it's one of the features that supports software engineering. However, constraint-checking routines can consume as much as 40% of a program's execution time. Some compilers detect certain constraint violations, such as illegal variable assignments, at compile time rather than postponing the discovery until runtime. This technique eliminates constraint-checking code from the runtime program and speeds the program's execution. Compilers can also evaluate constants, as well as expressions that compute values based on constants, at compile time. This feature saves code space and execution time. Some compilers can evaluate such expressions across separately compiled program units for even greater efficiency.

Many constraint checks can be eliminated without removing the safety net provided by the checks. For example, a program doesn't need to check constraints inside a loop if the loop parameters make the generation of an exception impossible. Thus, one constraint check at the start of the loop may suffice. In addition, Ada programs run much faster if you disable constraint-checking routines. You may be able to permanently disable constraint checking if your software testing has ensured that constraint violations aren't possible. Ada's "suppress" pragma lets you tell the compiler to omit certain types of constraint checking.

The optimizer can also speed a program's computations. Algebraic simplification or the application of deMorgan's theory often allow a compiler to reduce the strength of a computation by substituting a simple operation for a complex one. For example, a compiler might replace an operation that raises a variable to the second power with an expression that multiplies the variable by itself. Similarly, multiplication can often be replaced with addition ($2*X = X+X$). Boolean arrays can be packed so that logical operations occur a word at a time instead of a bit at a time. In some cases, this optimization can even reduce a loop to one instruction.

Reference

Gilinsky, Richard J and Sabina H Saib, "Design for High Performance," Proprietary Software Systems, Santa Monica, CA.

Even though the compilers must accommodate every Ada feature, few programmers use every facet of any programming language.

port the following software-engineering concepts:
- Top-down development
- Strong data typing
- Abstraction (data and actions)
- Information hiding and encapsulation
- Separation of specification from implementation
- Reusability
- Separation of physical realization from logical concepts
- Portability
- Modularity
- Readability.

Ada supports top-down program development through program subunits called "packages." A package delivers the capabilities of subprograms contained within the package to other portions of the program without revealing the inner details of those subprograms. In fact, packages can be compiled separately at different times, and the Ada compiler confirms that subprograms from another part of the program call a package's subprogram properly, by using the right number of parameters and the correct data types. Because only the package's interface is visible to the rest of the program, the overall program structure can be created without worrying about the detailed design of each package. Separate compilation of a package's interface specifications and its code body lets you create a high-level program design and construct the necestsary packages, postponing the packages' implementation details until later.

Strong data typing helps an Ada compiler ensure that the interfaces between two program units match, even if those units are separately compiled. Ada doesn't even let you add two integers unless they have the same precision. This feature prevents inadvertent mixing of data types and forces you to make all type conversions explicit, a rule that makes Ada code easier to maintain over the years. Consequently, you must declare a data type for every variable you use in an Ada program. The compiler won't provide you with default data types.

Abstraction allows you to hide the details of a program unit inside of the unit and provide a public description of the unit's function. Ada has two mechanisms for abstracting a program unit's actions: subprograms (functions and procedures) and packages. Ada's subprograms are not substantially different from the equivalent entities in other programming languages. However, packages and generics are novel Ada constructs. A package can contain any combination of data

Robotic parts carriers driven by Ada programs *in a new factory in Sweden help Volvo build automobiles. (Courtesy TeleSoft)*

types, descriptions, functions, and procedures. The Ada package lets you create a set of functions that operate on a special data type, such as complex numbers, that you define within the package. Ada's packages encourage you to create reusable code modules; the language's separate-compilation feature further enhances that programming style. Ada packages are essentially software components, and a business has sprung up in the Ada domain to create and market collections of independently developed Ada packages (statistics, thermal analysis, graphics, etc).

Generics create software templates

The generic package, or generic, takes the concepts of the Ada package one step further. A generic is a parameterized package that serves as a template for other modules. For example, you might create a stack package that knows how to create and manage stacks in memory. Without the generic, you'd need different packages to handle integer, floating-point, and character stacks. But the generic lets you create one generic package and then instantiate that package by using parameters to define the data type to be stored on the stack.

The Ada package also supports encapsulation and information hiding. These two characteristics help to keep a programmer's assumptions valid. Because Ada is designed to support multimillion-line programs, the strong protection mechanisms of encapsulation and information hiding are critical features of the language.

Encapsulation lets you gather information into a module and allow access to this information only in well-defined ways. The rest of your program cannot manipulate these encapsulated values except through the package calls you create. Without encapsulation, a module in a remote portion of a program might tinker with a package's critical values and cause the package

to generate erroneous results. Thus, encapsulation preserves the package programmer's assumptions regarding data integrity within the package.

The second protection mechanism, information hiding, prevents other program units from using intermediate values that are generated within the package. Without this feature, a remote portion of a program might use intermediate values that might not exist in the next package revision. Thus, information hiding prevents the creator of that remote piece of code from making assumptions about values in a package.

Ada packages also let you separate a module's specification from its implementation and compile them separately. This ability encourages top-down design because it lets you create and compile the module's specification as part of the high-level design process, and then return to the module later to complete the detailed coding. In addition, Ada packages promote reusability by forcing a programmer to document the package's interface in the specification.

Coupling to the physical machine

To promote portability, Ada's designers tried to create a language that is not specific to any machine. However, every program must eventually address the special characteristics of the machine running the software. In the form of representation specifications ("rep specs") and pragmas, Ada provides a bridge between the logical machine and the physical machine. Rep specs let you create special data types whose structures exactly match the physical machine's data structures. Thus, you can map your hardware's I/O registers and memory locations into Ada variables once through a rep spec, and then use the physical bits of the machine as logical variables throughout the rest of your program. Pragmas are compiler directives that can direct a compiler to make specific associations between Ada structures and the physical machine.

If the entire link between the Ada program and the physical machine exists through rep specs and pragmas, then the rest of the program is portable across a range of computing hardware. However, you don't get portability simply by using Ada to write programs. Ada provides the tools required to build portability into a program, but you'll still need to discipline yourself to confine machine-specific code to well-defined modules.

You can create nonmodular code with Ada if you work at it, but Ada clearly encourages a modular coding style. In addition, the language's requirement that you declare everything, including a package's interface specifications, enhances the readability of Ada programs. A determined programmer can use any language to write unreadable code, so a few rules for programming style are helpful.

Ada's language features make it an excellent choice for creating large programs, but Ada's specification also incorporates several aspects of a real-time, operating-system (OS) executive to enhance its use in developing embedded systems. The Ada runtime environment appears in **Fig 2** as classified by ARTEWG (the Ada Runtime Environment Working Group, sponsored by ACM SIGAda—the Ada special-interest group of the Association for Computing Machinery). The Ada runtime environment incorporates components that activate and terminate tasks, manage memory and I/O functions, keep track of time, and handle interrupts.

When you are choosing among competing Ada compilers for real-time application development, one of the first choices you must make is the type of runtime executive you want. You have three choices: First, you can pick an Ada development system that integrates a real-time executive written by the compiler vendor into the compiler's runtime library. Second, you can pick a development system that has been married to a commercial runtime kernel. Your third choice is writing your own real-time executive in Ada, assembly code, or another programming language.

Built-in Ada real-time executives employ Ada's tasking model to manage multiple tasks, using a priority scheme to schedule task execution. Ada's priority pragma lets you associate each task with a fixed prior-

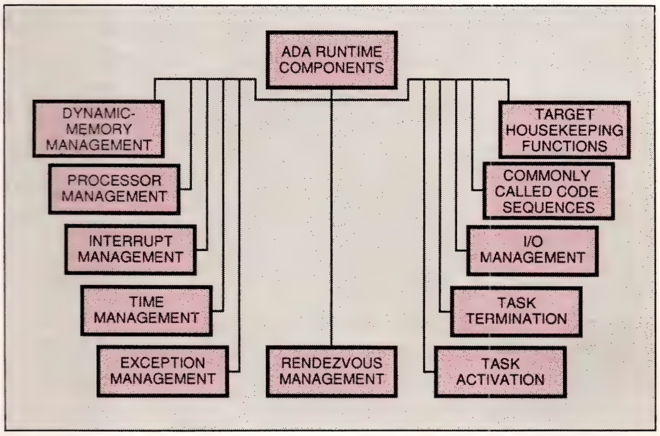


Fig 2—Ada's runtime environment manages several hardware resources *and also is responsible for task management. This classification was created by ARTEWG, the Ada Runtime Environment Working Group of ACM's SIGAda.*

Ada is a structured programming language, which primarily means that programs written in Ada make liberal use of the "begin" and "end" statements.

ity. That priority tells the scheduler which task to run if two or more tasks become unblocked at the same time. Tasks become blocked when waiting for a rendezvous (see **box**, "Synchronizing tasks through Ada's rendezvous"), when waiting for an Ada "delay" statement to expire, or when waiting for a dependent task to complete its execution.

The priority pragma can cause problems for real-time systems, because it permits only static (fixed) task priorities. Thus, if you have a mode-dependent system with tasks that vary in importance over time, the priority pragma won't let you change a task's priority to accommodate the mode shift. In addition, a task's priority, as assigned by the priority pragma, doesn't determine which task is chosen by a task server. Ada's specification requires server tasks to satisfy requests from other Ada tasks in FIFO order, ignoring task priority.

An Ada server task doesn't inherit the priority of the task it runs, and this characteristic may lead to priority inversion. During priority inversion, a lower-priority task pre-empts a higher-priority task. Because an Ada server doesn't inherit the priority of the task it's serving, it essentially transforms the priority of the task it's currently serving to the server's priority. For example, assume that an Ada program contains three tasks: task 1 with a priority of 20 (the larger the number, the higher the priority), task 2 with a priority of 18, and a server task with a priority of 15. If task 1 requests service from the server task, then task 1 effectively assumes a priority of 15 when the server task is satisfying task 1's request. During that time, task 2 can pre-empt the server task, thus pre-empting task 1, even though task 1 has the highest priority.

Runtime extensions increase efficiency

To compensate for these inadequacies of Ada's priority scheme, some Ada development-system vendors have created extensions to their runtime executives that allow Ada programs to work more efficiently in real-time applications. For example, DDC-I's runtime system lets you assign dynamic task priorities. It pro-

Synchronizing tasks through Ada's rendezvous

Ada allows you to break your program into multiple subprograms called tasks. These tasks are logically independent and can run concurrently. If you can divide your program into truly independent tasks, you need nothing more from the language. However, you often need a mechanism that allows tasks to cooperate by communicating and synchronizing with each other. Ada provides such a mechanism in its romantically named "rendezvous." The basic rendezvous process governs the interaction between a calling task and the called task.

An Ada task that wishes to send information to another task uses an "entry" statement to call the other task. The called task indicates its desire to receive information through an "accept" statement. If the calling task executes its entry statement first, it becomes blocked and stops executing until the called task executes its accept statement. Conversely, if the called task executes its accept statement before the calling task executes its entry call (a situation made possible by the tasks' concurrent execution), the called task becomes blocked and stops executing until the calling task executes the entry call. This process is the basic rendezvous mechanism, and it allows two tasks to synchronize by blocking one task until the other task reaches the rendezvous point.

You can also use the rendezvous mechanism to exchange information between the tasks through parameter passing. Parameters may be unidirectional, allowing one task to send information to another, or bidirectional, allowing the tasks to interchange information in both directions. The act of passing information between the tasks also synchronizes them.

Finally, you can create a task that will rendezvous with several other tasks by using the "select" statement to group several accept statements together. The select statement prevents the task from becoming blocked when the first accept statement is executed. Instead, the task becomes blocked by all of the accept statements defined within the select-statement block, and the task accepts the first entry call that arrives from any of the tasks involved in the rendezvous. Task servers use the select statement to rendezvous multiple client tasks.

Ada doesn't allow you to add two integers unless they have the same precision.

motes a server task's priority to the maximum of the server task's or the served task's priority, thus preventing priority inversions.

As designers continue to use Ada for a variety of projects, the features that the language needs to support real-time systems become more apparent. The ARTEWG has developed a Catalog of Interface Features and Options (CIFO) for Ada runtime environments, to promote a standard method for adding proposed real-time extensions to the language through packages and pragmas. The CIFO contains entries for features such as special delays, task identifiers, interrupt management, and fast-interrupt pragmas.

Fast interrupts cut overhead

The need for a fast-interrupt mechanism arises because Ada's conventional interrupt mechanism links an interrupt to an Ada task through the rendezvous mechanism (see **box**, "Synchronizing tasks through Ada's rendezvous"). Standard Ada tasks accept entry calls from other tasks in the program and incur a tremendous amount of overhead as the program's data structures are read and updated to preserve system state. The overhead of a rendezvous makes the conventional Ada interrupt mechanism too slow to be used for most real-time applications.

A fast-interrupt pragma labels the associated task as a fast-interrupt task and exempts that task from bookkeeping overhead. However, a fast-interrupt task must meet certain restrictions. First, the fast-interrupt task must use no more than a predefined amount of stack space. Also, the interrupt task's code must be straightforward and can't contain time-consuming statements such as delays or entry calls to other tasks. Finally, other program tasks can't call the fast-interrupt task—only the interrupt may activate this task. Fast interrupts can cut an interrupt-service routine's activation overhead by 50%.

Commercial runtime packages offer alternatives

In most cases, you can use a built-in runtime executive when Ada's tasking model works for your application. However, many designers of real-time systems are accustomed to other tasking models and prefer alternative communications mechanisms, such as semaphores. If you fit into this category, you may prefer to use a hybrid development tool that teams an Ada compiler with a standard, commercial runtime package. Several Ada packages incorporate real-time kernels from vendors such as Ready Systems, Industrial Programming Inc (Jericho, NY), and Wind River Systems (Emeryville, CA).

The RTAda packages from Ready Systems combine TeleSoft Ada compilers with ARTX, an enhanced version of the Ready Systems VRTX32 runtime kernel. ARTX incorporates the services needed to manage Ada tasks (create, delete, suspend, resume, and assign priority); a time-slicing (round-robin) scheduler; character I/O routines; timekeeping; interrupt services; memory allocation; and intertask communications services. If you have used Ready Systems' OS kernel in the past, ARTX's compatibility with VRTX32 makes it easier to convert programs written in C or assembly language, because the kernel calls don't change. This compatibility lets you incrementally convert previously written programs when time allows, or when you need to enhance an existing program.

Commercial real-time kernels such as ARTX give you explicit control over task scheduling. You can create, destroy, suspend, and resume tasks by using calls

How to get Ada aid

Tackling Ada is a very big project, but fortunately help is available. Several sources provide you with substantial amounts of information, often for free. The DoD operates the Ada Information Clearinghouse, which publishes a quarterly newsletter. For more information, write to AdaIC, Room 3D139, The Pentagon, Washington, DC, 20301, or call (703) 685-1477. You can also receive information from the AdaIC's computerized bulletin board by calling (202) 694-0215 or (301) 459-3865. The ACM sponsors the SIGAda users group, which publishes *Ada Letters*, a bimonthly newsletter; contact Dr Ben Brosgol at Alsys Inc. In addition, ACM SIGAda will sponsor the TRI-Ada conference at the Software Engineering Institute in Pittsburgh, PA, on October 23-26, 1989. This year, TRI-Ada will focus on real-world Ada applications. For further information, contact John Foreman at (412) 268-6217, or Charles B Engle, Jr at (412) 268-6525.

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to the kernel. Although Ada's rendezvous mechanism also provides this control, it relies on the interaction of two or more tasks. In addition, commercial real-time kernels give you several types of intertask-communication links, including mailboxes, binary event flags, queues, and semaphores, instead of Ada's single technique of passing parameters between tasks. These additional links let you tailor intertask communications by using the most efficient communications technique for your situation.

Unfortunately, you must accept a loss of portability when you use the extended services of a commercial real-time kernel. If you use these extensions, and then later move your program to another processor (using a different compiler), the runtime environment will be different, and those extended services may no longer be available. In that case, you would be forced to rewrite small or even large portions of your software.

You have another alternative if you need to extend Ada's runtime capabilities: You can write those extensions in Ada as part of your program. For example, if you need semaphores, you can write an Ada package that implements semaphores. Similarly, you can write your own task scheduler in Ada if you don't like Ada's priority scheme. Thus, if your application calls for a cyclic executive, you can write one in Ada as part of your program. Using Ada's own capabilities to extend the language lets you maintain portability across compilers and processors. However, the resulting code might be too slow for your application.

Fortunately, higher speed is the real-time Ada vendor's Holy Grail. These vendors realize that Ada won't become a widespread language unless the resulting code can run as fast as code generated with other programming languages. The common perception is that Ada is an inherently large and slow language when compared with a "fast and dirty" language such as C. However, several Ada-compiler vendors claim that the optimized code generated by their products can run as fast, or faster, than code generated by C compilers (**Fig 3**).

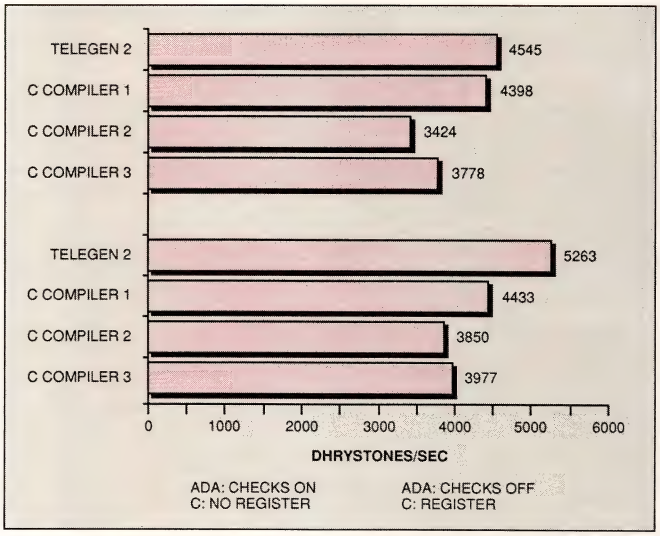

Fig 3—As compiler technology has improved, Ada vendors *are comparing the speed of their products to other languages known for their speed. For example, TeleSoft's Ada compiler for the Motorola 68000 µP family can exceed the performance of C compilers in the Dhrystone benchmark.*

Benchmarks may be helpful

When you start to compare the code generated by different development systems, you immediately descend into the gray world of benchmarks. Ada compilers must be validated before they can bear the name "Ada," but validation gives you no indication of performance. The Ada community has created many benchmark program suites that test compiler performance. Some benchmarks employ large programs to test the overall efficiency of a compiler, and other benchmark test suites use several small programs to focus on the performance of individual Ada features.

Some of the principal Ada benchmark test suites include the US government's Ada Compiler Evaluation Capability (ACEC); the PIWG (Performance Issues Working Group of ACM SIGAda, pronounced "piewig") benchmarks; the British government's Ada Evaluation System (AES); and various benchmark programs stored in the Ada Software Repository.

The ACEC test suite comprises 240 programs that perform more than 1000 tests. These tests focus on execution performance of the code generated by the compiler, and they also measure compile time and code size. The ACEC test suite is available to qualified DoD contractors from the Data Analysis Center for Software (Griffiss AFB, NY).

The PIWG constructed and maintains a suite of benchmark programs in the public domain. (For more information on the PIWG, contact Rob Spray, PIWG Tree, Box 850236, Richardson, TX.) The PIWG programs test the performance of Ada features such as clock resolution; task creation and rendezvous times; dynamic storage allocation; exception handling speed; procedure-call and constraint-checking overhead; and compilation speed. Many Ada-development-system

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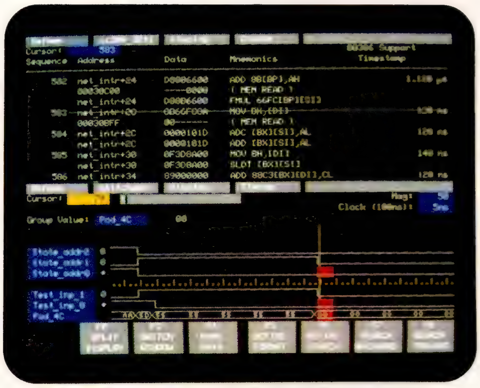

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Ada's definition also incorporates several aspects of a real-time, operating-system executive to enhance its use in developing embedded systems.

vendors provide the results of the PIWG benchmarks if you ask for them, but be careful not to make faulty comparisons; the benchmarks are run on a wide variety of processor architectures at differing clock speeds and with different memory wait states. These hardware differences can mask variations in compiler performance.

The British government developed the AES test suite in 1987 to measure compile- and execution-time performance, the quality of the generated code, the quality of the error and warning messages generated at compile time, and the capabilities of the Ada development system's debugger. The AES is distributed by the Information Technology Department of the British Standards Institute (Milton Keynes, UK).

The Ada Software Repository resides on a computer in the Defense Data Network. It is accessible to many DoD contractors and to certain universities through

Manufacturers of real-time Ada development systems

For more information on real-time Ada development systems such as those described in this article, circle the appropriate numbers on the Information Retrieval Service card or use EDN's Express Request service. When you contact any of the following manufacturers directly, please let them know you saw their products in EDN.

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CIRCLE NO 68

the Arpanet network. The repository contains source code, software components (packages), and educational material to support Ada development efforts, and it holds many benchmark test suites, including the PIWG programs.

For nearly a decade, the DoD and a sizable number of government contractors and software developers have pushed the development of Ada along the path to maturity. It is a fortuitous coincidence that Ada has ripened at about the same time that many engineers have started to use 32-bit μPs for real-time embedded systems. Hacking a few million lines of code is a contradiction in terms, and systems based on 32-bit processors can no longer be programmed in the style of their predecessors. For big programming jobs, you should consider Ada. EDN

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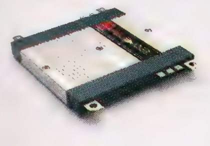

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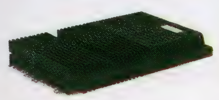

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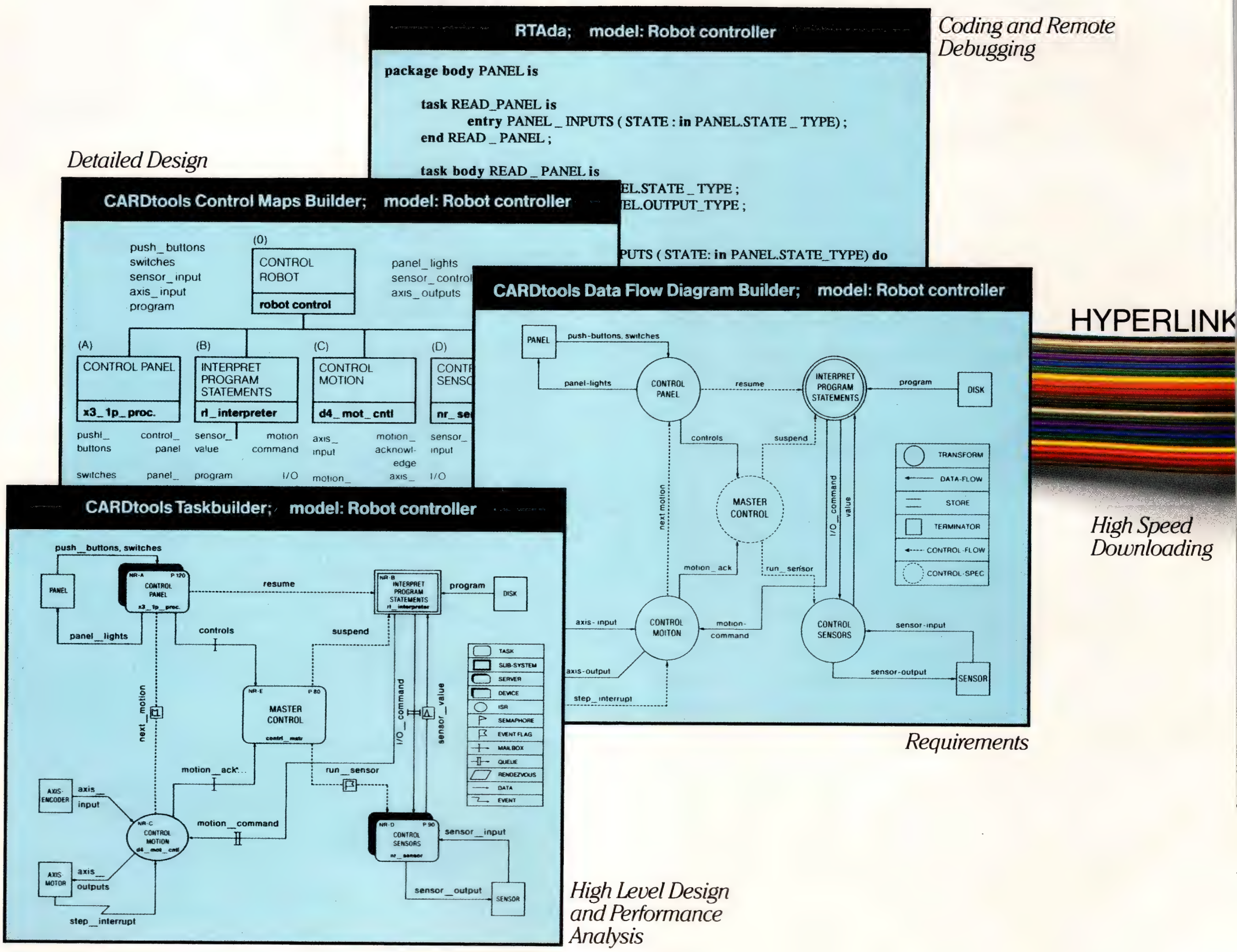

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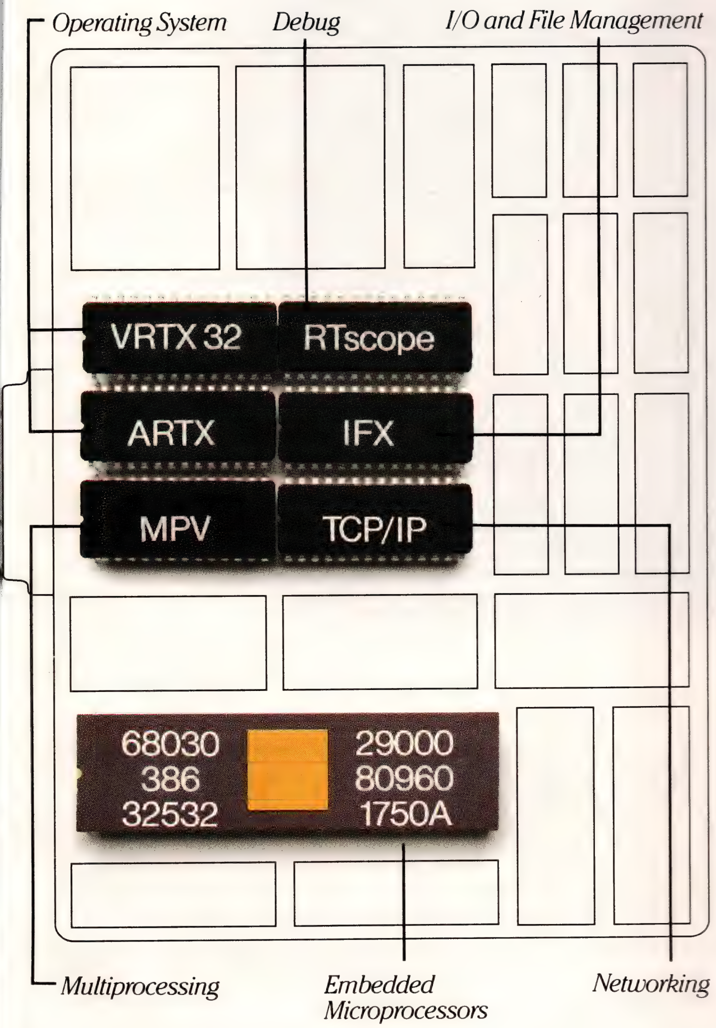

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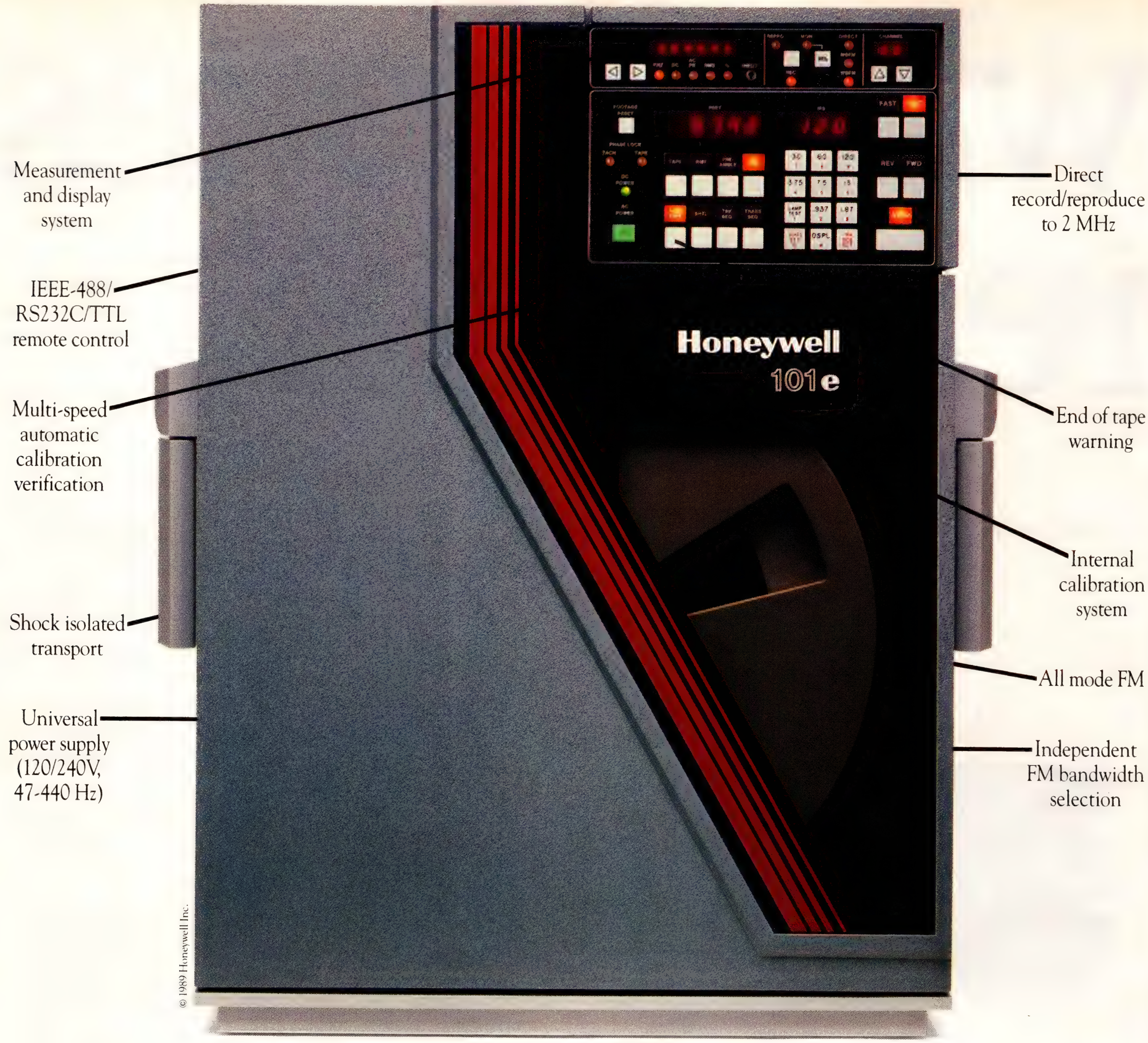

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CIRCLE NO 72

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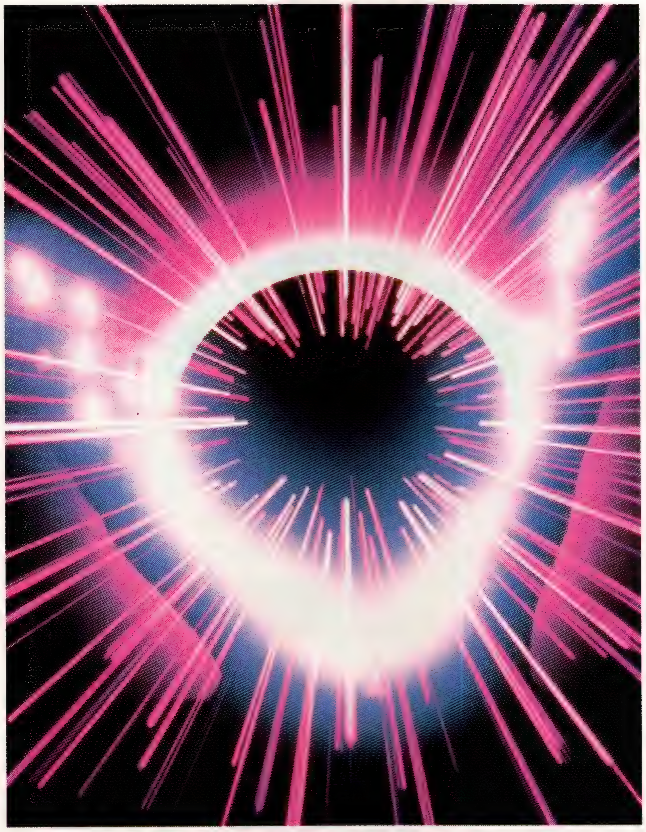

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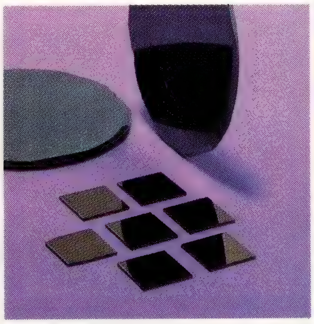

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Faraday rotation angle (deg.)	45±0.5	45±0.5
Insertion loss (dB/45°)*	≦0.3	<0.4
Change of Faraday rotation by temperature (deg./K)**	0.08	0.04
Extinction ratio (dB)*	>35	>35
Field for saturation magnetization (Oe)	~200	~700

* With anti-reflection coat   ** Wavelength at 1.3 μm

• Garnet LPE Films for magnetic sensor (0.8 μm)

Composition	$(RBI)_3Fe_5O_{12}$ R: Rare-earth elements
Verdet constant (deg./Oe)	2×10^{-2}
Insertion loss (dB/45°)*	<2~3
Field for saturation magnetization (Oe)	~1500

* With anti-reflection coat, magnetic garnet film = 30 μm.

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TROUBLESHOOTING

Analog Circuits

PART 7

Rely on semiconductor basics to identify transistor problems

Although transistors—both bipolars and MOSFETs—are immune to many problems, you can still have transistor troubles. Robust design methods and proper assumptions regarding their performance characteristics will steer you past the shoals of transistor disasters. After taking on 2-terminal devices in part 6, Bob covers these 3-terminal devices. Future parts will cover analog ICs.

Robert A Pease, *National Semiconductor Corp*

Transistors are wonderful—they're so powerful and versatile. With a handful of transistors, you can build almost any kind of high-performance circuit: a fast op amp, a video buffer, or a unique logic circuit.

On the other hand, transistors are uniquely adept at causing trouble. For example, a simple amplifier probably won't survive if you short the input to the power supplies or the output to ground. Fortunately, most op amps include forgiving features, so that they can survive these conditions. When the μA741 and the LM101 op amps were designed, they included extra transistors to ensure that their inputs and outputs would survive such abuse. But an individual transistor is vulnerable to damage by excessive forward or reverse current at its input, and almost every transistor is capable of melting. So it's up to us, the engineers, to design transistor circuits so that the transistors do not blow up, and we must troubleshoot these circuits when and if they do.

A simple and sometimes not so obvious problem is installing a transistor incorrectly. Because transistors have three terminals, the possibility of a wrong connection is considerably greater than with a mere diode. Small-signal transistors are often installed so close to a printed-circuit board that you can't see if the leads are crossed or shorted to a transistor's can or to a pc trace. In fact, I recall some boards in which the leads were often crossed and about every tenth transistor was the wrong gender—pnp where an npn should have been, or vice versa. I've thought about it a lot, and I can't think of any circuits that work equally well when you install a transistor of the opposite sex. So, mind your Ps and Qs, your Ps and Ns, and your 2N3904s and 2N3906s.

In addition to installing a transistor correctly, you must design with it correctly. First of all, transistors require input protection. Most transistors can withstand dozens of milliamperes of forward base current but will die if you apply only a few volts. One of my pet peeves has to do with adding protective components. MIL-HDBK-217 has always said that a circuit's reliability decreases when components are added. Yet when you add resistors or transistors to protect an

With a handful of transistors, you can build almost any kind of high-performance circuit, including fast op amps, video buffers, and unique logic circuits.

amplifier's input or output, the circuit's reliability actually improves. It just goes to show that you can't believe everything you read in a military specification. For a specific criticism of the notion of computing reliability per MIL-HDBK-217, see **Ref 1.**

Similarly, if you pump current out of the base of a transistor, the base-emitter junction will break down. This reverse current—even if it's as low as nanoamperes or very brief in duration—tends to degrade the beta of the transistor, at least on a temporary basis. So in cases where accuracy is important, find a way to avoid reverse biasing the inputs.

Transistors are also susceptible to ESD. If you walk across a rug on a dry day, charge yourself up to a few thousand volts, and then touch your finger to an npn's base, it will probably survive because a forward-biased junction can survive a pulse of a few amperes for a small part of a microsecond. But, if you pull up the emitter of a grounded-base stage, you risk reverse-biasing the base-emitter junction. This reverse bias can cause significant damage to the base-emitter junction and might even destroy a small transistor.

When designing an IC, smart designers add clamp diodes, so that any pin can survive a minimum of ±2000V of ESD. Many IC pins can typically survive two or three times this amount. These ESD-survival design goals are based on the human-body model, in which the impedance equals 100 pF in series with 1500Ω. In discrete transistors, whose junctions are considerably larger than the small geometries found in ICs, ESD damage may not be as severe. But in some cases, ESD damage can still happen. Delicate RF transistors such as 2N918s, 2N4275s, and 2N2369s sometimes blow up "when you just look at 'em" because their junctions are so small.

Other transistor-related problems arise when engineers make design assumptions. Every beginner learns that the V_{be} of a transistor decreases by about 2 mV per degree Celsius and increases by about 60 mV per decade of current. Don't forget about the side effects of these rules, or misapply them at extreme temperatures. Don't make sloppy assumptions about V_{be}s. For instance, it's not fair to ask a pair of transistors to have well-matched V_{be}s if they're located more than 0.1 in. apart and there are heat sources, power sources, cold drafts, or hot breezes in the neighborhood. Matched pairs of transistors should be glued together for best results.

I've seen people get patents on circuits that don't

Photographs by Peggi Willis

A curve-tracer can help you discern the difference *between a "good" transistor and a "bad" one. It can also help resolve the shape of the voltage-current curve of any nonlinear component.*

even work based on misconceptions of the relationships between V_{be} and current. It's fair to assume that two matched transistors with the same V_{be} at the same small current will have about the same temperature coefficient of V_{be}. But you wouldn't want to make any rash assumptions if the two transistors came from different manufacturers or from the same manufacturer at different times. Similarly, transistors from different manufacturers will have different characteristics when going into and coming out of saturation, especially when you're driving the transistors at high speeds. In my experience, a components engineer is a very valuable person to have around and can save you a lot of grief by preventing unqualified components from confusing the performance of your circuits.

Another assumption engineers make has to do with a transistor's failure mode. In many cases, people say that a transistor, like a diode, fails as a short circuit or in a low-impedance mode. But unlike a diode, the transistor is normally connected to its leads with relatively small lead-bond wires; so if there's a lot of energy in the power supply, the short will cause large currents to flow and vaporize the lead bonds. As the lead bonds deteriorate, the transistor will ultimately fail as an open circuit.

It's nice to design with high-beta transistors, and, "if some is good, more's better." But, as with most things in life, too much can be disastrous. The h-parameter, h_{rb}, equals $\Delta V_{be}/\Delta V_{cb}$ with the base grounded,

and many engineers have learned that as beta rises, so does h_{rb}. As h_{rb} rises, the transistor's output impedance decreases; its Early voltage falls; its voltage gain decreases; and its common-emitter breakdown voltage, BV_{ceo}, may also decrease. (The Early voltage of a transistor is the amount of V_{ce} that causes the collector current to increase to approximately two times its low-voltage value, assuming a constant base drive. V_{Early} is approximately equal to $(1/h_{rb}) \times 26$ mV.) So, in many circuits there is a point where higher beta simply makes the gain lower, not higher.

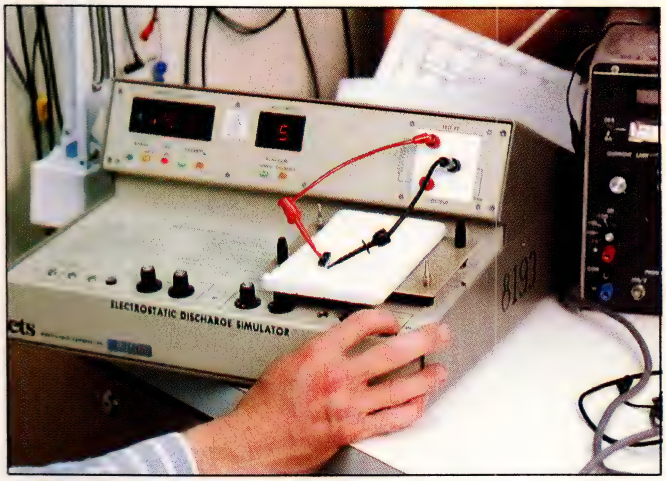
Another way to increase beta is to use the Darlington connection; but the voltage gain and noise may degrade, the response may get flaky, and the base current may decrease only slightly. When I was a kid engineer, I studied the ways that Tektronix made good use of the tubes and transistors in their mainframes and plug-ins. Those engineers didn't use many Darlingtons. To this day, I keep learning more and more reasons not to use Darlingtons or cascaded followers. For many years, it's been more important for many circuits to have matched betas than for them to have sky-high betas. You can match betas yourself or buy four or five transistors on one monolithic substrate, such as a monolithic transistor array.

One of the nice things about bipolar transistors is that their transconductance, g_m, is quite predictable. At room temperature, $g_m = 38.6 \times I_C$. Since the voltage gain is defined as $A_V = g_m \times Z_L$, computing it is often a trivial task. You may have to adjust this simple equation in certain cases. For instance, if you include an emitter-degeneration resistor, R_e, the effective transconductance falls to $1/(R_e + g_m^{-1})$. A_V is also influenced by temperature changes, bias shifts in the emitter current, hidden impedances in parallel with the load, and the finite output impedance of the transistor.

For a given operating current, field-effect transistors normally have much poorer g_m than bipolar transistors do. You'll have to measure your devices to see how much lower. Additionally, the V_{gs} of FETs can cover a very wide range, thus making them hard to bias.

Also be aware that although the transconductance of a well-biased transistor is quite predictable, beta usually has a wide range and is not nearly as predictable. So you have to watch out for adverse performance if the beta is too low or too high and causes shifts in your operating points and biases.

JFETs became popular 20 years ago because you could use them to make analog switches with resistances of 30Ω and lower. JFETs also made good op amps with lower base currents than bipolar devices, at least at moderate or cool temperatures. The BiFET process made it feasible to make JFETs along with bipolars on a monolithic circuit. It's true that the best BiFET inputs are still slightly inferior to the best bipolar ones in terms of voltage-offset temperature coefficient, long-term stability, and voltage noise. But these BiFET characteristics keep improving because of improved processing and innovative circuit design. As a result, BiFETs are very close to bipolar transistors in terms of voltage accuracy and offer the advantage of low input current.

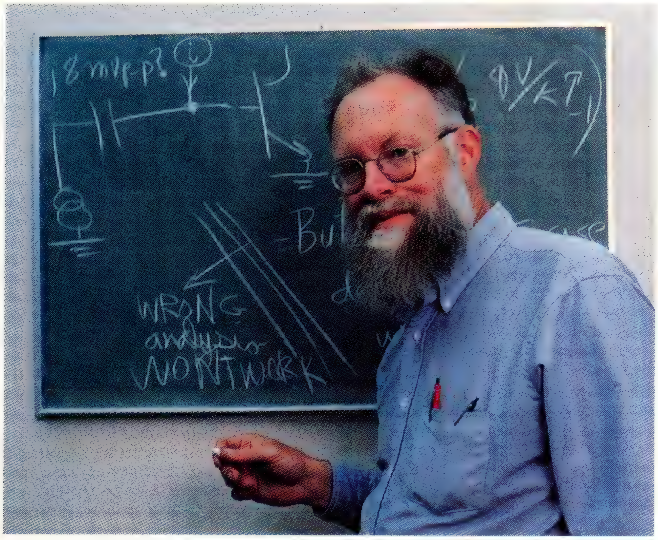


When you hit a component or circuit with a pulse of ESD, *you can never be sure what kind of trouble you'll get—unless you've already tested it with an ESD simulator.*

I recall working on a hybrid circuit that had some JFETs whose gate connections were supposed to be through the back of the dice. I found that some of the dice didn't have proper metallurgical processing, which caused some strange behavior. Initially, the gate acted as if it were connected and would act that way for a long period of time. Then, the gate would act like an open circuit with as much as 1V of error between the actual gate and the bottom of the die. The gate would remain disconnected until a voltage transient restored the connection for another week! The intermittency was awful because nothing would speed up the 1-week cycle-to-failure time. So, we had to go back and add definite lead bonds to the gate's bond pad on the top of the chip, which we had been told was unnecessary. Ouch!

When designing hybrids, you need to make sure to

Transistors are powerful and versatile, but they're also uniquely adept at causing trouble.



***Using equations to analyze circuits** can sometimes help you define a problem. But if the equations are inapplicable, they do a lot more harm than good. This circuit is a version of a patented circuit that was cleverly designed to the highest levels of confidence using equations. The fact that it doesn't work is a mere footnote—except to the engineer who has to troubleshoot it.*

connect the substrate of a chip to the correct dc level. The bottom of a FET chip is usually tied to the gate, but the connection may be through a large and unspecified impedance. You have to be a pretty good chemist or metallurgist to be sure that you don't have to add a bond to the gate's metal. A bipolar-transistor die's substrate is the collector. Most linear and digital IC substrates are tied to the negative supply. Exceptions include the LM117 and similar adjustable positive regulators—their substrate is tied to V_{out}. The LM196 voltage regulator's substrate is tied to the positive supply voltage, V_s, as are the substrates of the MM74HC00 family of chips and most of the dielectrically isolated op amps from Harris. So, be aware of your IC's substrate connection. If an LM101AH op amp's metal can bumps against ground or V_s, you have a problem. Similarly, you shouldn't let an HA2525's case bump against ground or $-V_s$.

MOSFETs are widely used in digital ICs but are also very popular and useful in analog circuits, such as analog switches. Op amps with MOSFET inputs do well in the general-purpose op-amp market. MOSFETs have a bad reputation for excessive noise, but new devices, such as the LMC662, demonstrate that clean processing can cure the problem, thus making MOSFETs competitive with BiFETs. Just be careful not to let ESD near the inputs. MOSFETs do have protection diodes and may be able to withstand 800V, but they can't survive 2000V. If you work with unprotected devices, such as the 3N160, you must keep the pins securely shorted until the device is soldered into its pc board in which the protection diodes are already installed. I do all of that and wash the transistor package with both an organic solvent and soap and water. And, I keep the sensitive gate circuits entirely off the pc board by pulling the gate pin up in the air and using point-to-point wiring. Air, which is a superior dielectric, is also a good insulator **(Ref 2)**. So far, I haven't had any blown inputs or bad leakages—at least nothing as bad as 10 fA.

On the other hand, when using CMOS digital ICs, I *always* plug them into live sockets; I *never* use conductive foam; and I *never* wear a ground strap on my wrist. And I've *never* had any failures—with one exception. One time I shuffled across a carpeted floor and pointed an accusatory finger at a CMOS IC. There was a small crack of ESD—probably 5000V—followed by a big SNAP as the IC blew out and crowbarred the entire power supply. Since ESD testing is done with the power OFF, if you did some tests with the power ON, you might get some messy failure modes like the one I just mentioned. Always be wary of any devices that manufacturers claim are safe from ESD.

Power transistors may hog current

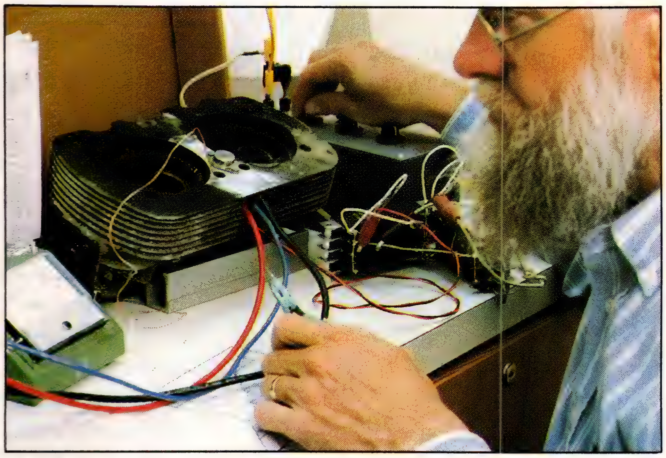
As you build a bipolar transistor bigger and bigger, you may be tempted to go to extremes and make a huge power transistor. But there are practical limitations. Soon, the circuit capacitances cause oppressive drive requirements, and removing the heat is difficult. Still, no matter how big you build power transistors, people will find a use for them. Their most severe problem is secondary breakdown, which is what happens when you drive a transistor outside its safe operating area.

When you operate a power transistor at very high currents and low voltages, the emitter resistance of the device—which includes the resistance of the emitter metal and the inherent emitter resistivity—can cause enough $I \times R$ drop to force the entire emitter and its periphery to share the current. Now, let's halve the current and double the voltage. The amount of dissipation is the same, but the $I \times R$ drop is cut in half. Now continue to halve the current and double the voltage. Soon you'll reach a point where the ballasting **(Fig 1)** won't be sufficient, and a hot spot will develop at a high-voltage point. The inherent decrease of V_{be}

causes an increase of current in one small area. Unless this current is turned OFF promptly, it will continue to increase unchecked. This "current hogging" may cause the area to melt or crater. The designers of linear ICs use ballasting, cellular-layout, and thermal-limiting techniques, all of which can prevent harm in these cases (**Ref** 3). Discrete transistors may someday include these features.

Fortunately, many manufacturers' data sheets include permitted safe-area curves at various voltages and for various effective pulse widths. So, it's possible to design reliable power circuits with ordinary power transistors. The probability of an unreliable design or trouble increases as the power level increases, as the adequacy of the heat sink decreases, and as the safety margins shrink. For example, if the bolts on a heat sink aren't tightened enough, the thermal path degrades and the part can run excessively hot.

High temperature *per se* doesn't cause a power transistor to fail. But, if the drive circuitry was designed to turn a transistor ON and only a base-emitter resistor is available to turn it OFF, then at a very high temperature, the transistor will turn itself ON and there will be no adequate way to turn it OFF. However, I once applied a soldering iron to a 3-terminal voltage regulator and then went to answer the phone. When I came back the next day, I discovered that the TO-3 package was still quite hot—300°C, which is normally recommended for only 10 seconds. When I cooled it off, the regulator ran fine and met spec. So, the old dictum that high temperature will necessarily degrade reliability is not always true. Still, it's a good practice not to get your power transistors that hot and to have a base drive that can pull the base OFF if they do.



When using high-power amplifiers, *there are certain problems you just never have if you use an extremely large heat sink. This heat sink's thermal resistance is lower than 0.5°C/W.*

You can also run into problems if you tighten the screws on the heat sink too tight or if the heat sink under the device is warped or has bumps or burrs or foreign matter on it. If you tighten the bolt too much, you'll overstress and warp the tab and die attach. Overstress may cause the die to pop right off the tab. The insulating washer under the power transistor can crack due to overstress or may fail after days or weeks or months. Even if you don't have an insulating washer, overtorqueing the bolts of plastic-packaged power

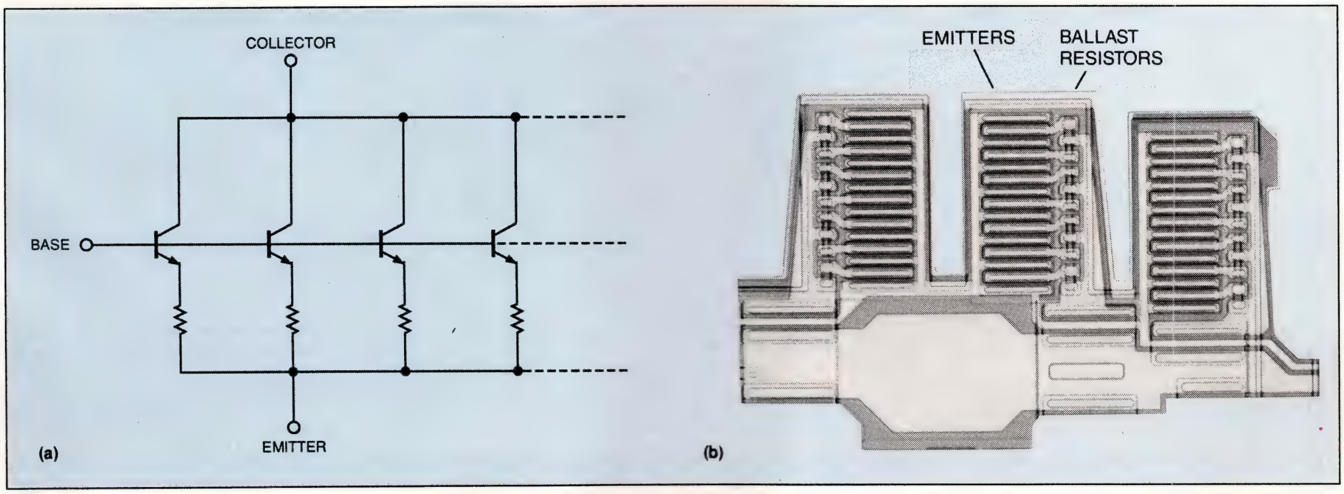


Fig 1—Ballast resistors, also known as sharing resistors, *are often connected to the emitters of a number of parallelled transistors* ***(a)*** *to help the transistors share current and power. In an integrated circuit* ***(b)****, the ballast resistors are often integrated with adjacent emitters. (Photo of National Semiconductor Corp's LM138)*

Mind your Ps and Qs and your Ps and Ns; don't mistakenly insert a pnp transistor in place of an npn, or vice versa.

transistors is one of the standard ways to mistreat and kill these devices. Why does the number 10 inch-pounds max, 5 typ, stick in my head? Because that's the spec the Thermalloy man gave me for the mounting bolts of TO-220 packages.

Apply the 5-second rule

Your finger is a pretty good heat detector—just be careful not to burn it with high voltages or very hot devices. A good rule of thumb is the 5-second rule: If you can hold your finger on a hot device for five seconds, the heat sink is about right, and the case temperature is about 85°C. If a component is too hot to touch, dot your finger with saliva and apply it to the hot object for just a fraction of a second. If the moisture dries up quickly, the case is probably around 100°C; if it sizzles instantaneously, the case may be as hot as 140°C. Alternatively, you can buy an infrared imaging detector for thousands of dollars, and you won't burn your fingers.

Fabrication structures make a difference

Another thing you should know when using bipolar power devices is that there are two major fabrication structures: the epitaxial base and the single diffused **(Fig 2) (Ref 4)**. Transistors fabricated with the single-diffused structure are more rugged and have a wide safe-operating area. Epitaxial-base devices feature faster switching speeds but aren't as rugged as the single-diffused types. A good way to compare the two types is to look at the data sheets for the Motorola 2N3771 and MJ3771. The MJ3771 epi-base device has a current-gain bandwidth 10 times greater than the 2N3771 single-diffused device. The MJ3771 also has a switching speed faster than the 2N3771 when used as a saturated switch, but the 2N3771 has a considerably larger safe area if used for switching inductive loads. You can select which of these characteristics you prefer and order the part according to the specific number.

But there isn't always a clear correlation between the part number and its fabrication structure. For example, the popular 2N3055 is available in both epi-base and single-diffused versions. Since both versions meet and exceed the JEDEC specs, you could end up with either type. If you breadboard with one type and then start building in production with the other, you might suddenly find that the bandwidth of the device has changed by a factor of 10 or that the safe area doesn't match that of the prototypes.

Fortunately, there are ways to order the 2N3055 you want. If you want to buy an ordinary 2N3055—one that meets but does not exceed the device's JEDEC specs—the die will be about 90 mils on a side, the bandwidth will be about 2 MHz, and it will have a nominal safe area because it is an epi-base device. If you want to buy a really gutsy 2N3055, order a 2N3055H from RCA or SGS-Thomson. RCA calls the device's construction hometaxial, which is similar to single diffused. The part's die is about 180 mils on the side, so—obviously—the 2N3055H costs more than the

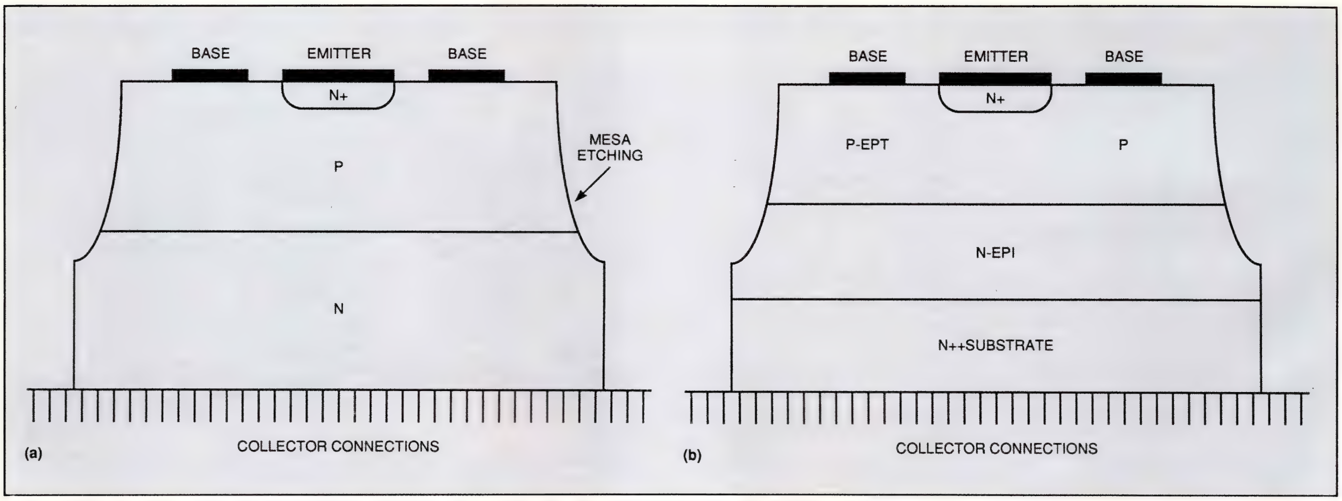


***Fig 2—The characteristics of power transistors** depend on their fabrication structure. In the single-diffused structure **(a)**, n-type dopants are diffused simultaneously into the front and back of a thin p-type wafer. This structure produces rugged transistors with wide safe operating areas. The more modern epitaxial-base transistor **(b)** takes advantage of the properties of several different epitaxial layers to achieve higher beta, faster speed, lower saturation, smaller die size, and thus, lower cost. Both structures involve mesa etching, which accounts for the slopes at the die edges.*

Transistors require protection against excessive forward and reverse base current and electrostatic discharge.

2N3055. The 2N3055H's bandwidth is only 0.3 MHz, but its safe area is considerably bigger than that of the ordinary 2N3055. Thus, 2N3055Hs are recommended for switching inductive loads.

Be careful not to confuse these epitaxial or single-diffused devices with planar power devices, such as the 2N5039 **(Fig 3)**. The 2N5039 has a frequency response around 60 MHz but a considerably smaller safe area than those of the epitaxial and single-diffused devices. As with smaller transistors, such as the 2N2222 and 2N3904, planar devices tend to oscillate at high frequencies. The judicious use of ferrite beads in their emitter or base leads is often required for stable linear operation.

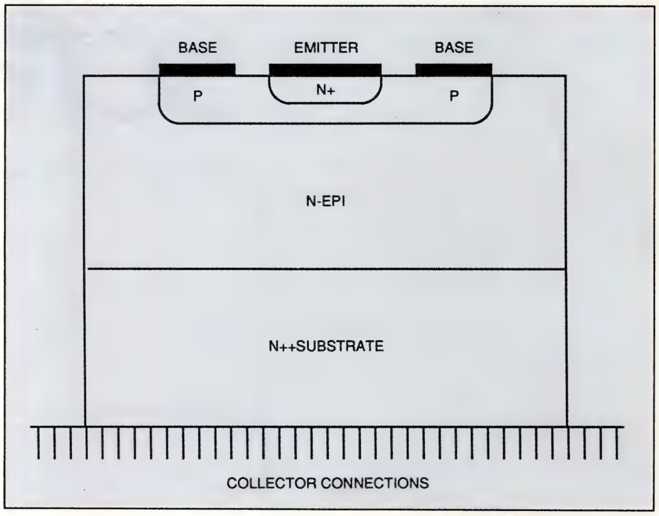


***Fig 3—Planar power transistors can achieve very small geometries,** small base-widths, and high frequency responses, but they're less rugged than the single-diffused and epitaxial-base types.*

Power-circuit design requires expertise

For many power circuits, your transistor choice may not be as clear-cut as in the previous examples. So, be careful. Design in this area is not for the hotshot just out of school—there are many tricky problems that can challenge even the most experienced designers. For example, if you try to add small ballasting resistors to ensure current sharing between several transistors, you may still have to do some transistor matching. This matching isn't easy. You'll need to consider your operating conditions; decide what parameters, such as beta and V_{be}, you'll match; and figure out how to match different manufacturers' devices. Such design questions are not trivial.

When the performance or reliability of a power circuit is poor, it's probably not the fault of a bad transistor. Instead, it's quite possibly the fault of a bad or marginal driver circuit or an inadequate heat sink. Perhaps a device with different characteristics was inadvertently substituted in place of the intended device. Or perhaps you chose the wrong transistor for the application.

A possible scenario goes something like this. You build 10 prototypes, and they seem to work okay. You build 100 more, and half of them don't work. You ask me for advice. I ask, "Did they ever work right?" And you reply, "Yes." But wait a minute. There were 10 prototypes that worked, but the circuit design may have been a marginal one. Maybe the prototypes didn't really work all that well. If they're still around, it would be useful to go back and see if they had any margin to spare. If the 10 prototypes had a gain of 22,000, but the current crop of circuits has gains of 18,000 and fails the minimum spec of 20,000, your design is not really a failure. It's not that the circuit isn't working at all, it's just that your expectations were unrealistic.

After all, every engineer has seen circuits that had no right to work but did work—for a while. And then when they began to fail, it was obviously just a hopeless case. So, which will burn you quickest, a marginal design or marginal components? That's impossible to say. If you build in some safety margin, you may survive some of each. But you can't design with big margins to cover every possibility, or your design will become a monster.

MOSFETs avoid secondary breakdown

When it comes to power transistors, MOSFETs have certain advantages. For many years, MOSFETs have been available that switch faster than bipolar transistors with smaller drive requirements. And MOSFETs are inherently stable against secondary breakdown and current hogging because the temperature coefficient of I_{ds} vs V_{gs} is inherently stable at high current densities. If one area of the power device gets too hot, it tends to carry less current and thus has an inherent mechanism to avoid running away. This self-ballasting characteristic is a major reason for the popularity of MOSFETs over bipolar transistors. However, recent criticism points out that when you run a MOSFET at high enough voltages and low current, the current density gets very small, the temperature coefficient of I_{ds} vs V_{gs} reverses, and the device's inherent freedom from current hogging may be lost **(Ref 5)**. So at high volt-

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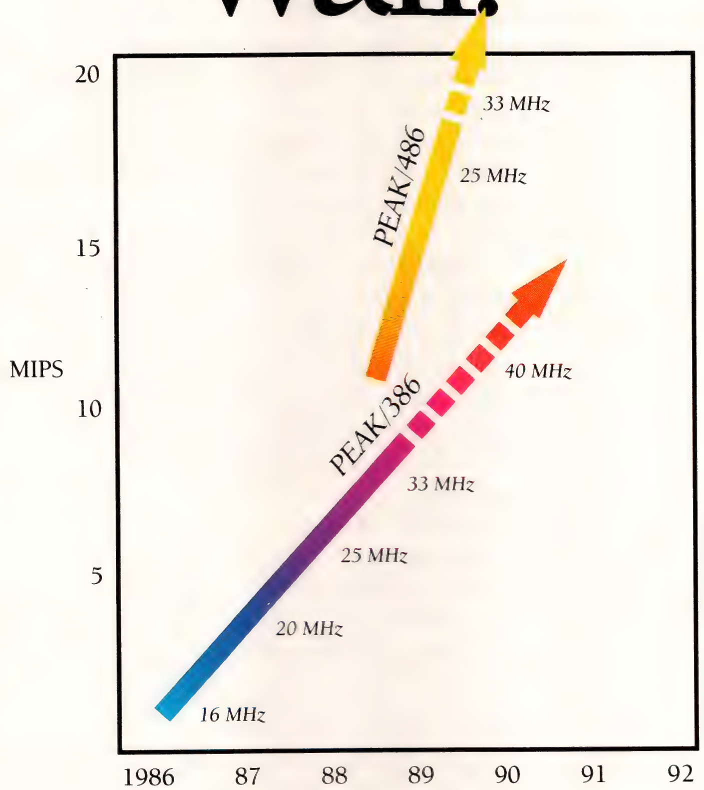

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Don't be too quick to blame circuit problems on a transistor; the designer may have made some sloppy assumptions or had false performance expectations.

ages and low current densities, watch out for this possibility.

The newer power MOSFETs are considerably more reliable and less expensive than the older devices. Even though you may need a lot of milliamps to turn the gate ON or OFF quickly, you don't need a lot of amps to hold it ON like you do with a bipolar transistor. You can turn the newer devices OFF quicker, too, if you have enough transient gate drive current available.

However, MOSFETs are not without their trouble spots. If you dissipate too many watts into a MOSFET, you can melt it just as you can melt a bipolar device. If you don't overheat a MOSFET, the easiest way to cause a problem is to forget to insert a few dozen or hundred ohms of resistance or a ferrite bead right at the gate lead of the device. Otherwise, these devices have such high bandwidths that they can oscillate at much higher frequencies than bipolar transistors.

For example, the first high-fidelity, all-MOSFET audio amplifier I ever saw blew up. It worked okay in the lab, but some misguided engineer decided that if a bandwidth of 5 Hz to 50 kHz was good, then 0.5 Hz to 500 kHz was better. Consequently, when the speaker cables were extended from 10 feet to 20 feet for a demonstration, the amplifier broke into a megahertz-region scream and promptly went up in smoke because of the lack of damping at the sources. I was told that after a minor redesign the amplifier was perfectly reliable. The redesign involved cutting the bandwidth down to a reasonable level, adding some ballasting in the sources, and tying antisnivet resistors directly to the gate pins. (Note: A snivet is a nasty, high-frequency oscillation originally found in vacuum-tube TV sets.)

As with bipolar transistors, MOSFETs are very reliable if you don't exceed their voltage, current, or temperature ratings. Dissatisfaction with a device's reliability or performance usually stems from the drivers or the related circuitry. Most MOSFETs have a maximum V_{gs} rating of just 20 or 25V. A MOSFET may temporarily survive operation with 30 or 50V on the gate, but it's not safe to run it up there forever. If you apply excessive gate voltage, gradual gain or threshold degradation may occur. So—please—don't. Also, power MOSFETs are not quite as rugged as bipolars when it comes to surviving ESD transients. A common precaution is to add a little decoupling, clamping, or current-limiting circuitry, so that terminals accessible to the outside world can withstand ESD.

DMOS FETs are so easy to apply that we usually forget about the parasitic bipolar transistor that lurks in parallel with them. If [dV/dt] is too large at the drain, the drain junction is avalanched at too high a current and voltage, or the transistor gets too hot, the bipolar device turns ON and dies an instant death due to current hogging or an excursion from its safe operating area.

But I'm spoiled rotten. I'm accustomed to linear ICs, which have protection transistors built right in, so most of the transistor troubles are left to the IC designer. Discrete designs are appropriate and cost-effective for many applications, but the availability of linear ICs—especially op amps—eases your design task considerably. Next time, we'll discuss the ins and outs and innards of op amps. EDN

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Author's biography

For information about Bob Pease, see the ***box****, "Who is Bob Pease, anyway?" on page 148 of the January 5, 1989, edition of EDN.*

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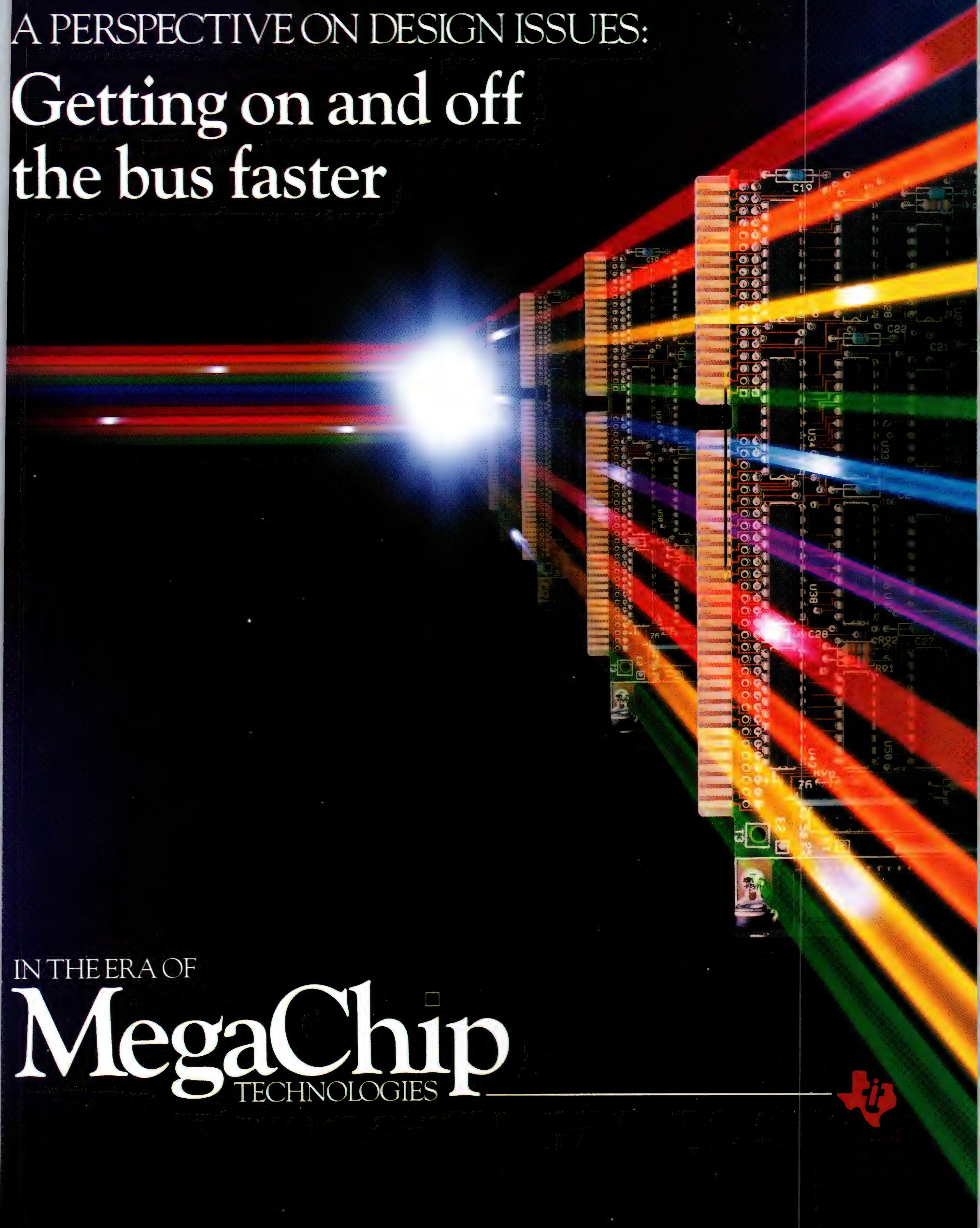

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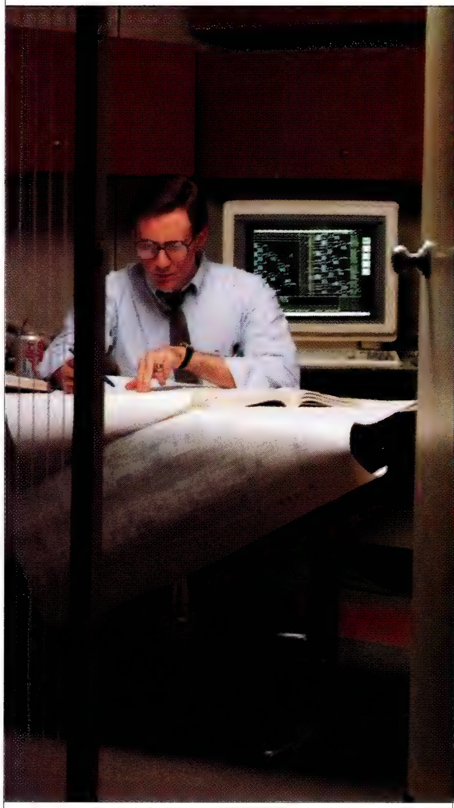

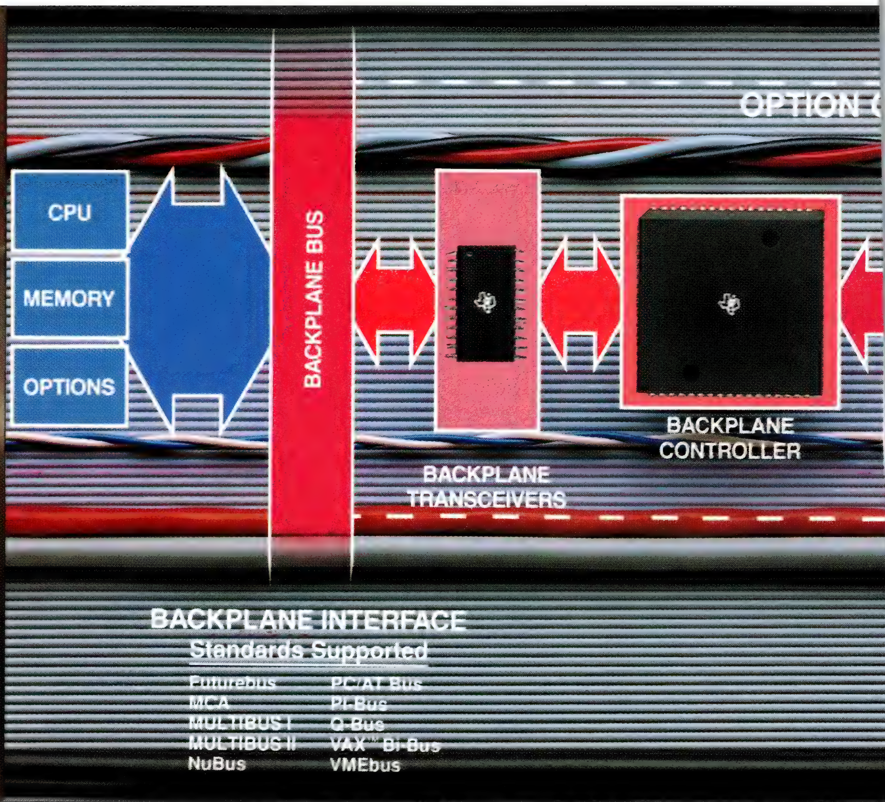

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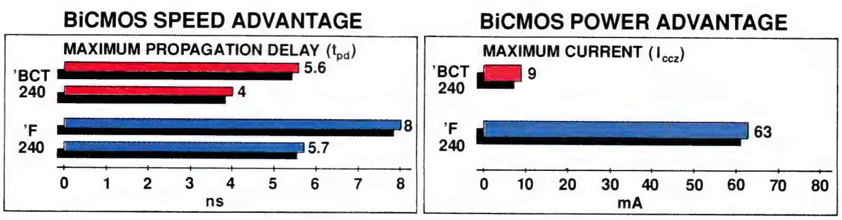

The BiCMOS lead over bipolar is proven by this comparison between TI's '74BCT240 and a comparable advanced bipolar standard device. Typical propagation delay of TI's BiCMOS part is faster (*left*) while power dissipation is less (*right*).

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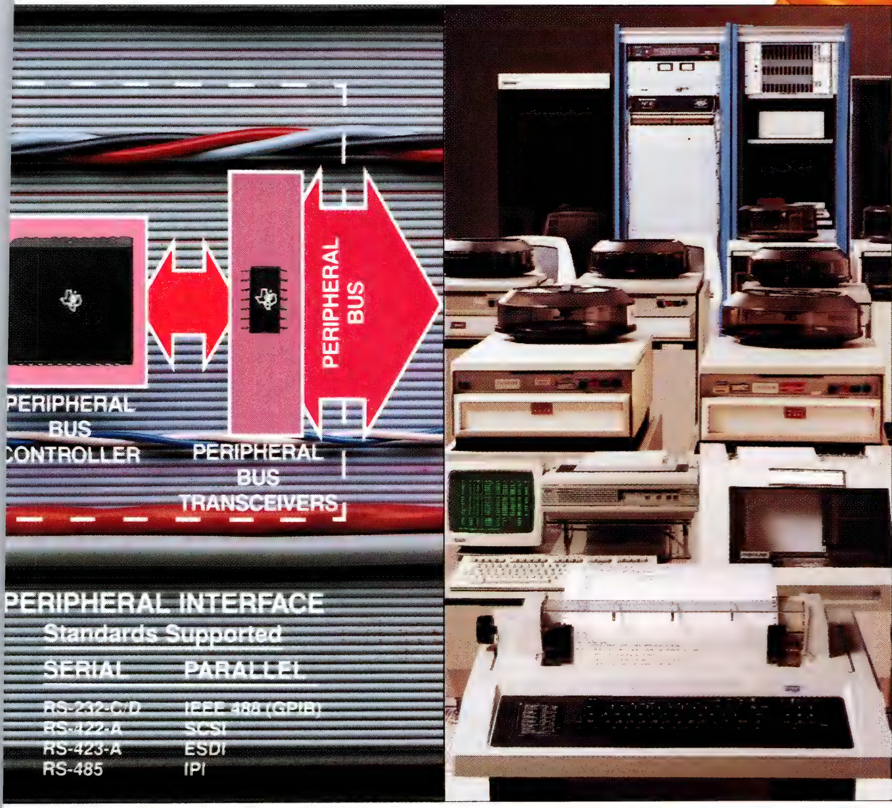

ICs. To complete the implementation, TI offers a series of innovative standard and ASIC control devices. Use of TI's leadership bus interface devices can help shorten system design cycles.

drive current you need, and total system power savings can be as high as 25% (*see charts*).

There are more than 60 members in our BiCMOS family, including 8-, 9-, and 10-bit latches, buffers, drivers, and transceivers. The family is also available in military versions.

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High-performance peripheral interfaces

Peripheral bus interface design decisions revolve around trade-offs between line length, data rate, and noise immunity.

Where data rates are low and line lengths are short, as with the popular RS-232-C/D standard, the major concern is power savings. However, relatively high voltages (30 V) prevent the use of standard CMOS devices. Your answer lies with TI's Linear BiCMOS family.

Included are low-power versions of industry-standard quad drivers and receivers (SN75C188/89). Driver/receiver combinations, ranging from single to quad combinations (SN75C1154), substantially cut package count.

This BiCMOS technology will also allow us to provide charge pump circuitry for single 5-V operation.

Where data rates are high and line lengths are long, as the newer peripherals demand, noise can become a major problem. It is overcome by the use of differential drive. Typically, the major application requirement is higher speeds at, ideally, lower power.

For example, disk drives using ESDI, IPI, or SCSI interfaces will benefit from TI's SN75ALS17X devices conforming to RS-422-A and/or RS-485 standards. These chips are fabricated using our unique IMPACT™ processing that delivers up to 50% greater speed compared to competing products with as much as a 30% power reduction.

IMPACT processing is also behind the unmatched speed of our SN75AS030 RS-422 dual driver/receiver. Typical propagation delays are only 6 ns. ■

No matter which of TI's innovative devices you choose to improve speed, cut power, and reduce real estate at the media interface, the complete bus interface requires another element — controllers. *For details on how TI is addressing your needs in this area, turn the page.*

High-performance controllers make system design easier.

While the majority of physical-layer devices—those used to implement backplane and peripheral interfaces—transmit data, your system design also requires a device to regulate the flow of that data through the bus interface. To do the job, TI offers a series of controllers that simplify and shorten your task while cutting chip count and improving overall system throughput.

Simplified NuBus design

TI has taken much of the work out of NuBus™ design by introducing the industry's first standard NuBus interface devices. They are the SN74ACT2440 NuBus Controller and the SN74BCT2420 NuBus Registered Transceiver.

A typical implementation, using two 16-bit transceivers and one 32-bit controller (*see below*), replaces as many as 45 discrete devices. Compared to a discrete approach, this solution uses 60% less board space and 90% less power.

Because the necessary logic is embedded within the controller, design cycle time is reduced significantly.

A low-power UART

There is now more need than ever for low-power RS-232 interfaces. Our TL16C450 Universal Asynchronous Receiver/Transceiver (UART), made with CMOS process technology, is an excellent choice for desktop applications and is especially suited for use in laptop/battery-powered units.

A flexible SCSI controller

Available soon, our SCSI controller (designed to conform to ANSI X3.131-1986 specifications) will deliver data rates of 3 Mbytes/s (asynchronous) and 5 Mbytes/s (synchronous).

Unique byte-stacking control logic will allow interface to 16-, 24-, and 32-bit buses. The TI controller will also provide powerful multiphase SCSI commands, including automatic handling of save-data pointer to minimize interrupts to the host processor. Dual 32-byte FIFOs will provide smooth, efficient buffering between processor and DMA ports.

Customized controllers, too

The NuBus and UART controllers are available as part of our ASIC standard-cell library.

In addition, TI offers TGC100 Gate Arrays and TSC500 Standard Cells as part of our ASIC family which allows you to build the precise chip functions you need. ■

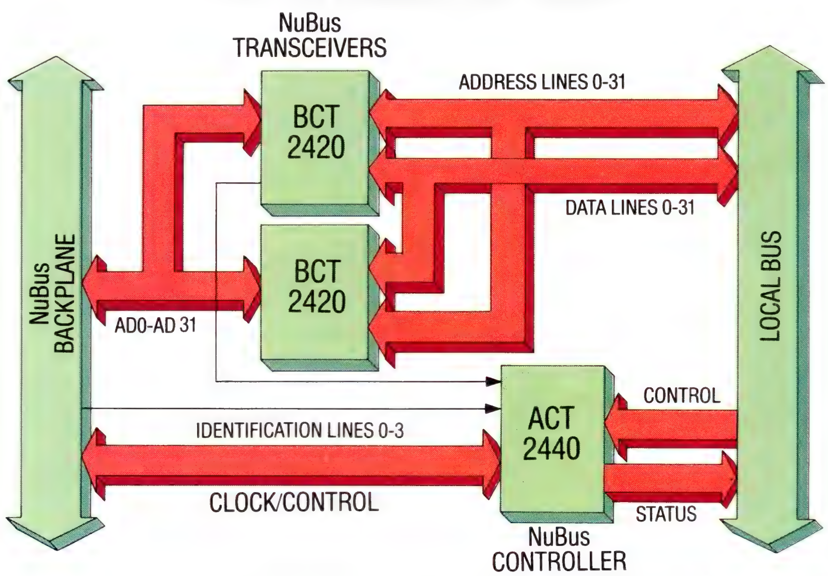
System complexity and the future

As systems become more and more complex, the need will emerge for combining the functionality of controllers and physical-layer devices on a single chip. To that end, TI is applying its acknowledged expertise in physical-layer devices to the design and development of such advanced control-level ICs.

System complexity also brings with it the need for simulation models to make design easier and faster. As a result, we already have simulation models available for more than 1,300 TI devices, including BiCMOS bus interface and ACL logic devices.

Another issue is the increasing difficulty and expense of testing boards in complex systems. Consequently, TI supports the JTAG/IEEE P1149.1 standard with the development of standard products and ASICs having on-chip test cells, as well as with development support software and device models on several leading workstations. ■

TI's 32-bit NuBus Interface Solution



Major space savings are realized by using one TI SN74ACT2440 controller and two SN74BCT2420 transceivers to complete a full 32-bit NuBus master/slave interface. As many as 45 discrete logic devices are replaced, realizing significant reductions in board space, power consumption, and design cycle time.

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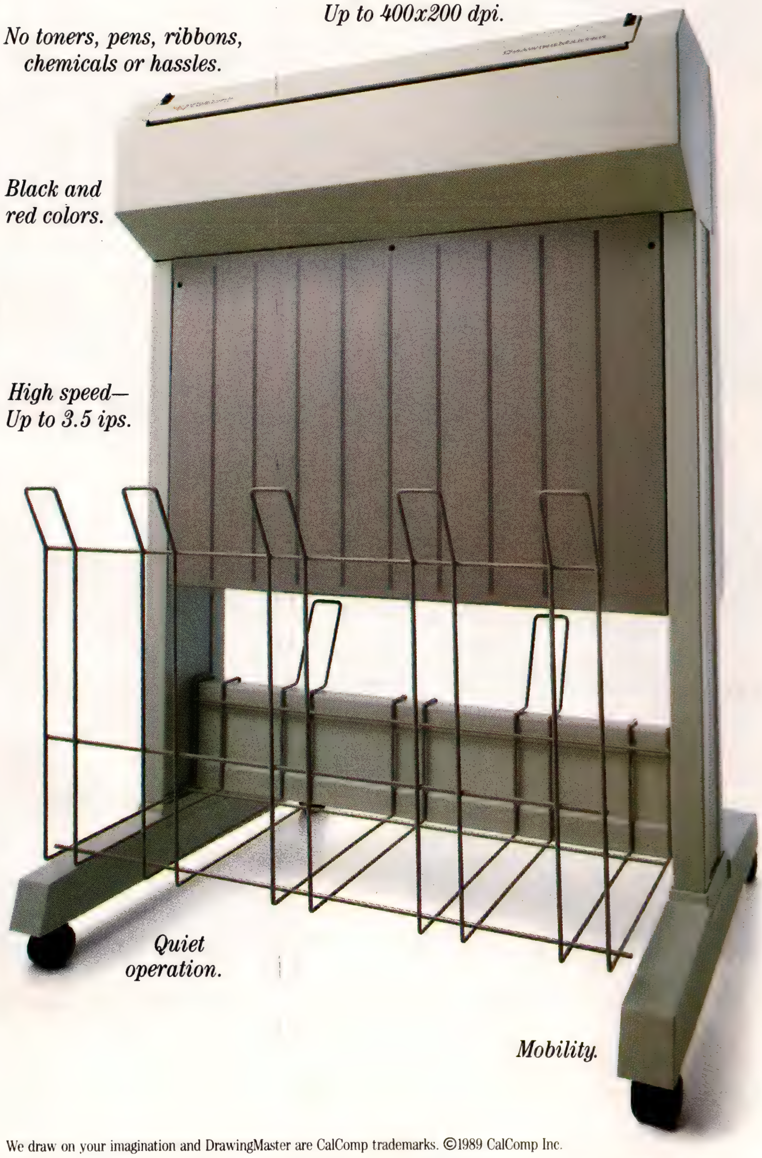

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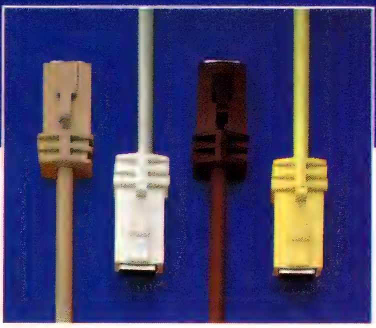

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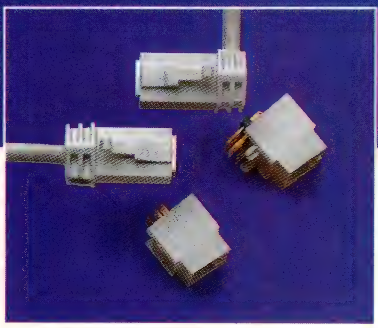

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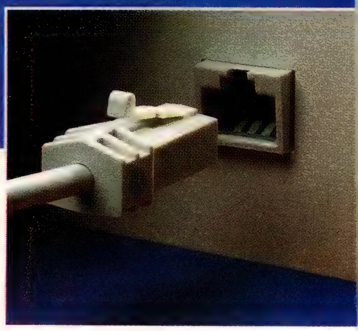

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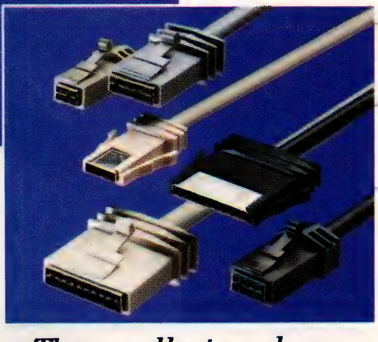

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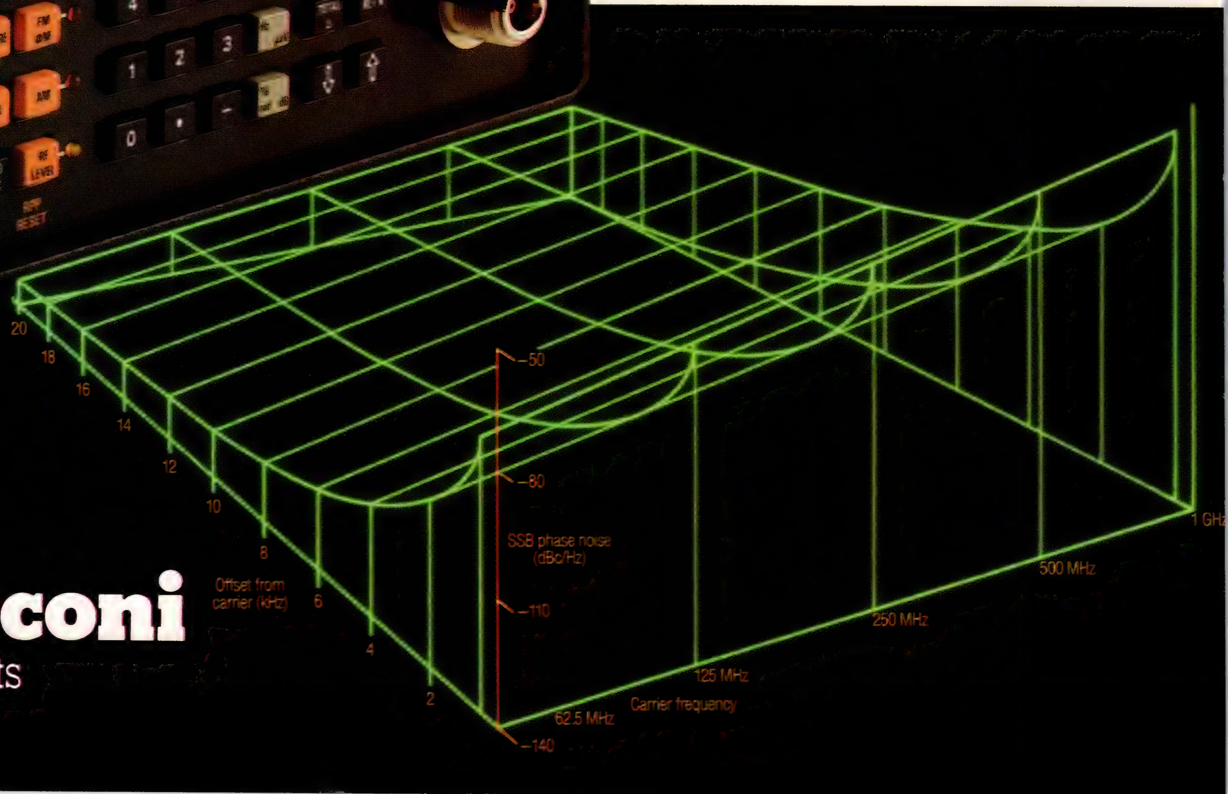

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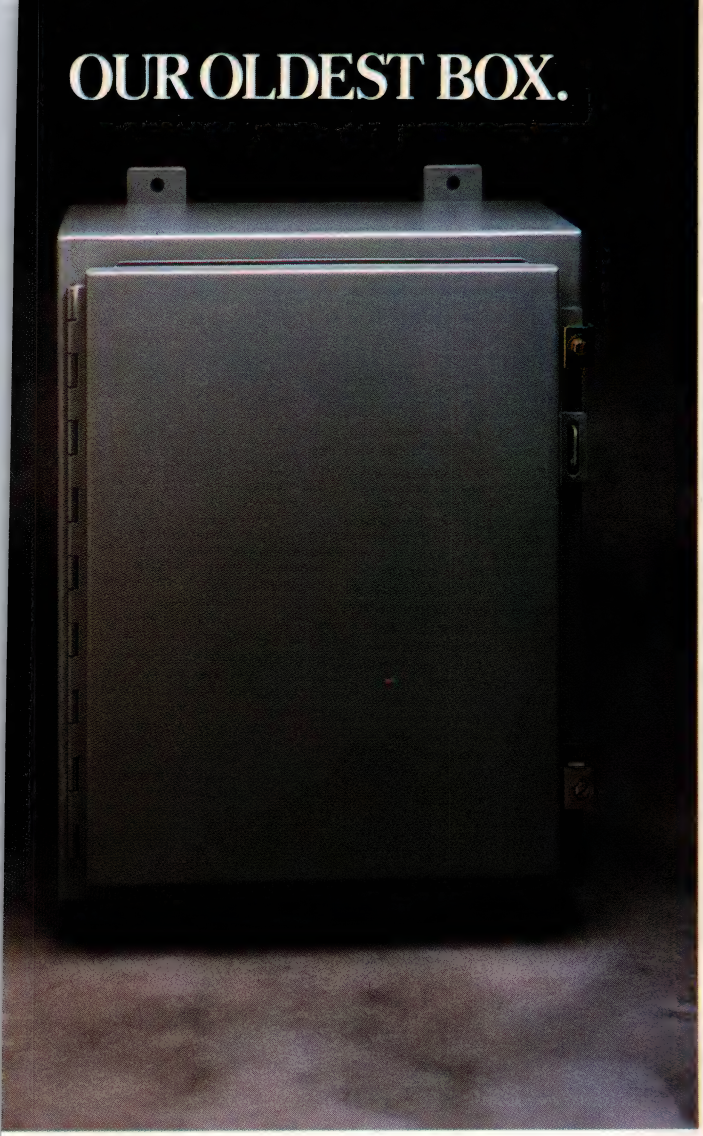

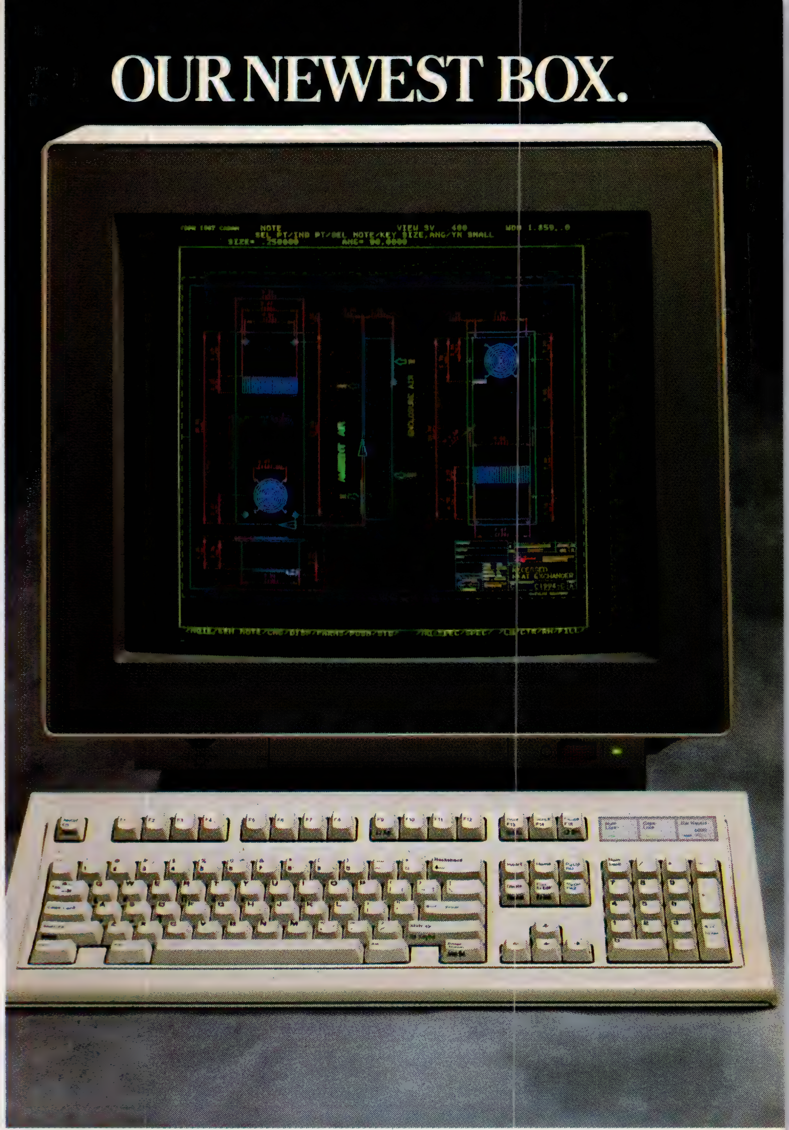

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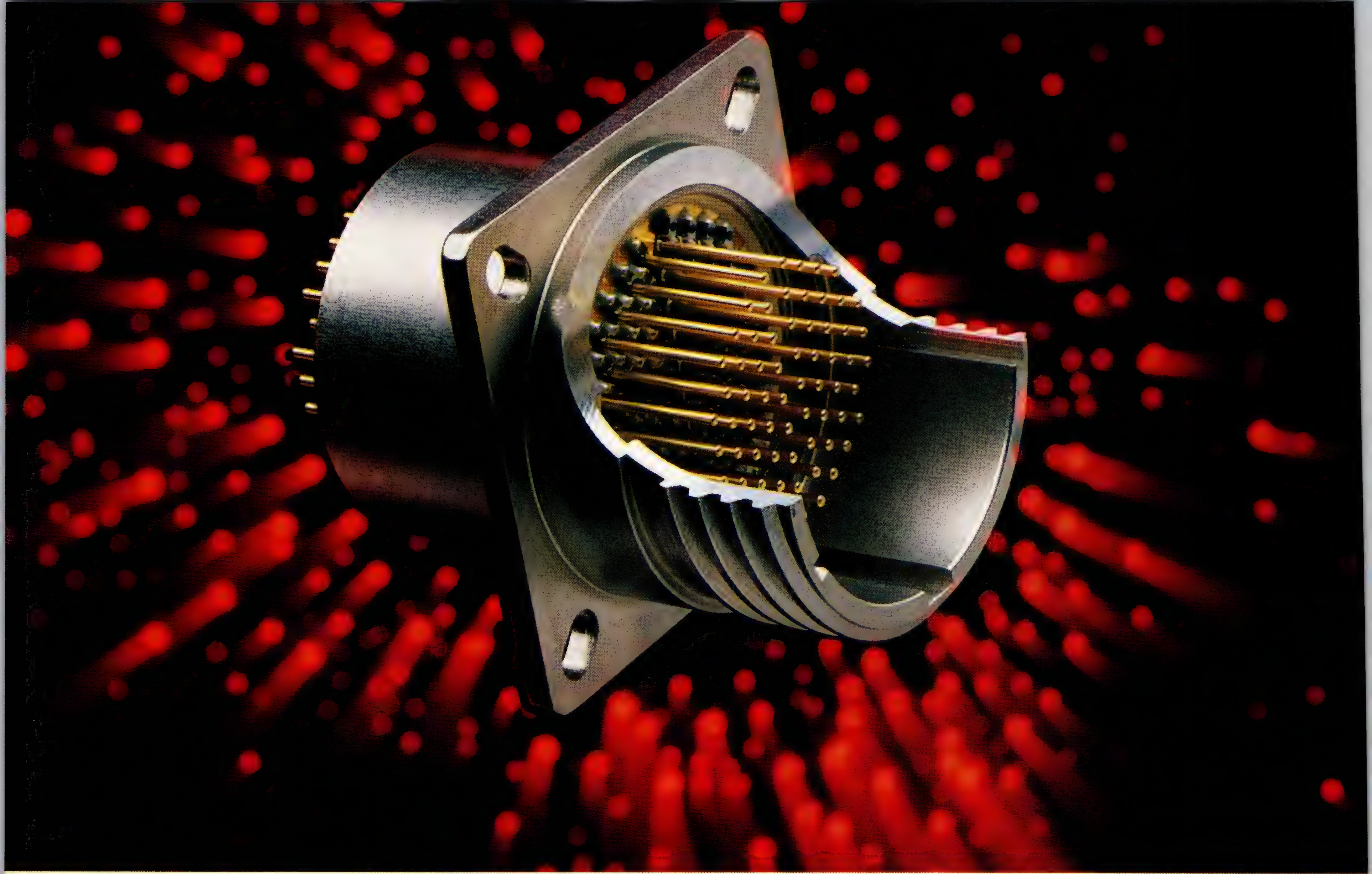

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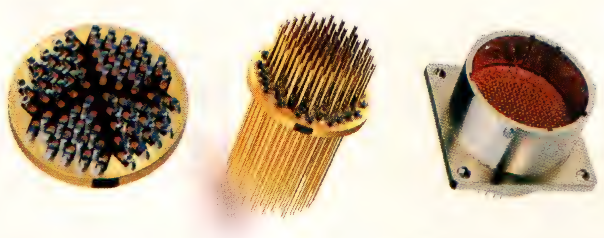


Astute designs improve efficiencies of linear regulators

Linear voltage regulators outperform switching-type devices in many applications, but they have one major drawback—poor efficiency. By employing careful design techniques and using new regulator components, you can greatly improve efficiencies.

Jim Williams, *Linear Technology Corp*

Although switching-type voltage regulators are gaining in popularity, linear voltage regulators are still popular devices. Linear regulators are easy to implement and have much better noise and drift characteristics than switchers. In addition, they function with standard magnetics, are easy to compensate, don't radiate RF, and have fast response times. However, linear regulators are saddled with one major drawback—poor efficiency. As a result, they're associated with high operating temperatures and large heat-sink requirements. Linear regulators cannot compete with switching regulators in these performance characteristics, but by using certain design techniques and new linear-regulator devices, you can achieve significantly better results than you might think is possible.

A basic way to improve the efficiency of linear regulators is to minimize the input-to-output voltage across the regulator. The smaller this term is, the lower the power loss. Manufacturers refer to the minimum input-output voltage necessary to support regulation as the dropout voltage. Different regulator design techniques and technologies offer different regulator performance (see **box,** "Achieving a low dropout voltage"). Conventional 3-terminal linear regulators typically have a 3V dropout, but newer devices feature a 1.5V dropout at 7.5A and a 0.05V dropout at 100 μA. You can use these new regulators to achieve relatively high efficiencies. However, the overall regulator performance depends greatly on the quality and amplitude of the input signal.

Stable inputs ease problems

Lower dropout voltage leads to significant power savings when the input voltage is relatively constant—that is, when a linear regulator postregulates a switching-power-supply output **(Fig 1).** Here, feedback to the switching regulator stabilizes the main output, A. Output A usually supplies most of the power available from **Fig 1**'s circuit. Therefore, the power demands at the B and C outputs have relatively little effect on the amount of energy in the transformer.

Because of this action, the input voltages to the B and C regulators are relatively constant. Judicious design enables the regulators to run at or near their dropout voltage, regardless of the loading or switcher input voltage. Low-dropout regulators thus save considerable power.

Unfortunately, not all applications boast a stable input voltage. **Fig 2** illustrates a classic situation in which

You can improve the efficiency of a linear regulator by minimizing the input-to-output voltage across the device.

the ac line drives the linear regulator through a step-down transformer. A 90 to 140V ac swing (brownout to high-line range) causes a proportionate change at the regulator input. The efficiencies of standard regulators versus low-dropout devices can vary considerably under such circumstances.

A low-dropout regulator has much higher efficiency on its 5V main output, where dropout figures can be a significant percentage of the output voltage. An efficiency comparison at a 15V output still favors the low-dropout regulator, although the gain in efficiency is not as great as that of a standard regulator. A look at power dissipation under the same output conditions shows that a low-dropout regulator requires less heat-sink area than a normal regulator to maintain the same die temperature. Input voltage variations have a deleterious effect on the efficiencies of both regulators, but a low-dropout regulator clearly cuts power losses.

Fig 3 shows a way to minimize regulator input variations even though the ac line has a wide voltage swing. This preregulator circuit combined with a low-dropout regulator provides high efficiency but still retains the desirable characteristics of a linear regulator.

This circuit servo controls the firing point of the SCRs to stabilize the LT1086 input voltage. IC_1 compares a portion of the LT1086's input voltage to the LT1004 reference. The amplified difference voltage at IC_1's output drives the inverting input of IC_{2B}. The circuit then compares IC_{2B}'s output to a line-synchronous ramp derived by IC_{2A} from the rectified secondary of the main transformer, T_1.

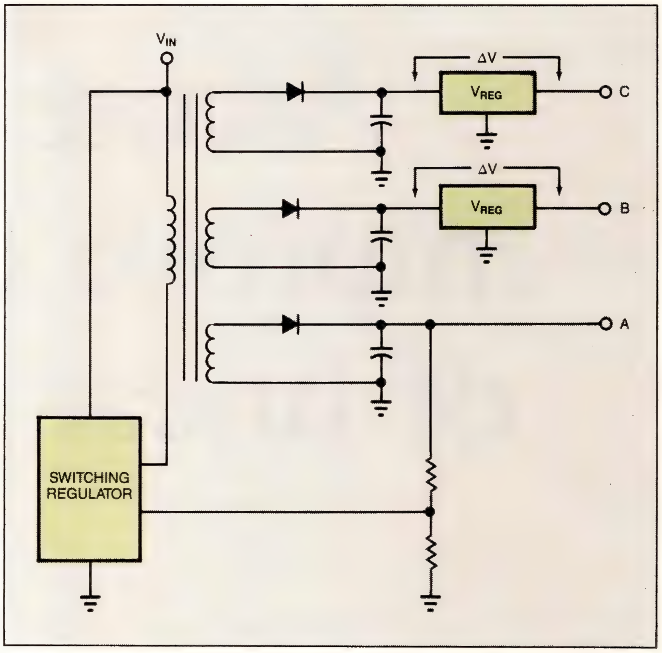


Fig 1—You can realize significant power savings *in applications in which the input voltage is relatively constant. In this circuit, a linear regulator postregulates a switching-power-supply output.*

The pulse output from IC_{2B} fires the appropriate SCR to develop a current flow from the transformer through L_1. This current flow charges the 4700-μF capacitor. When the transformer output drops low enough, the SCR commutates and charging stops. On

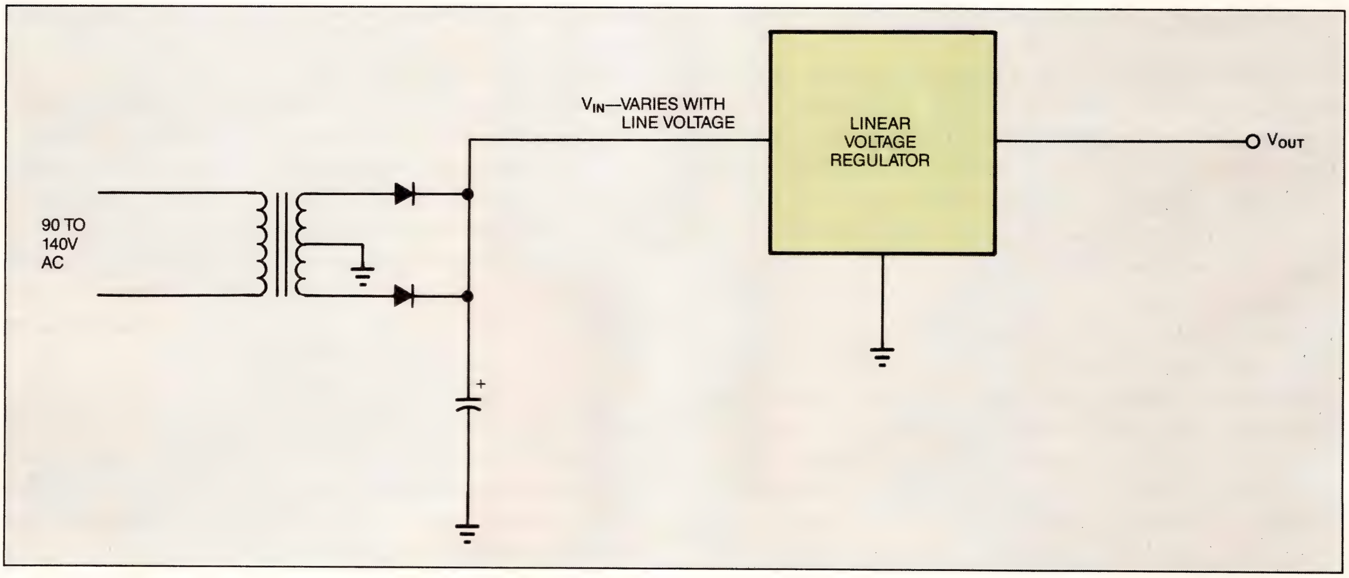


Fig 2—Achieving high efficiencies is difficult *when the input to the linear regulator varies in proportion to any line-voltage changes.*

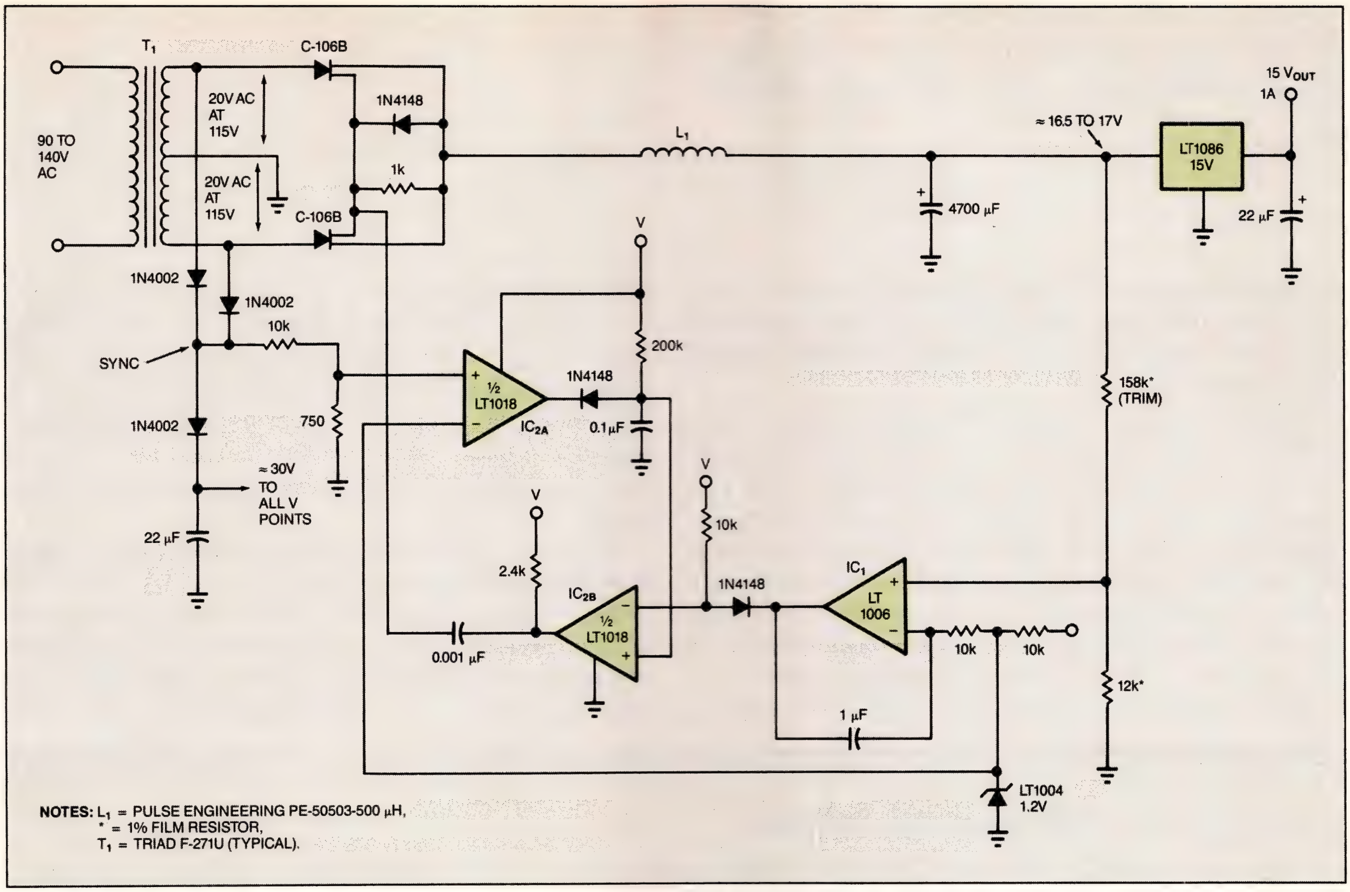


Fig 3—**There are ways to eliminate regulator input variations,** *even those with wide ac-line variations. This circuit provides high efficiency and retains all the desirable characteristics of linear regulators.*

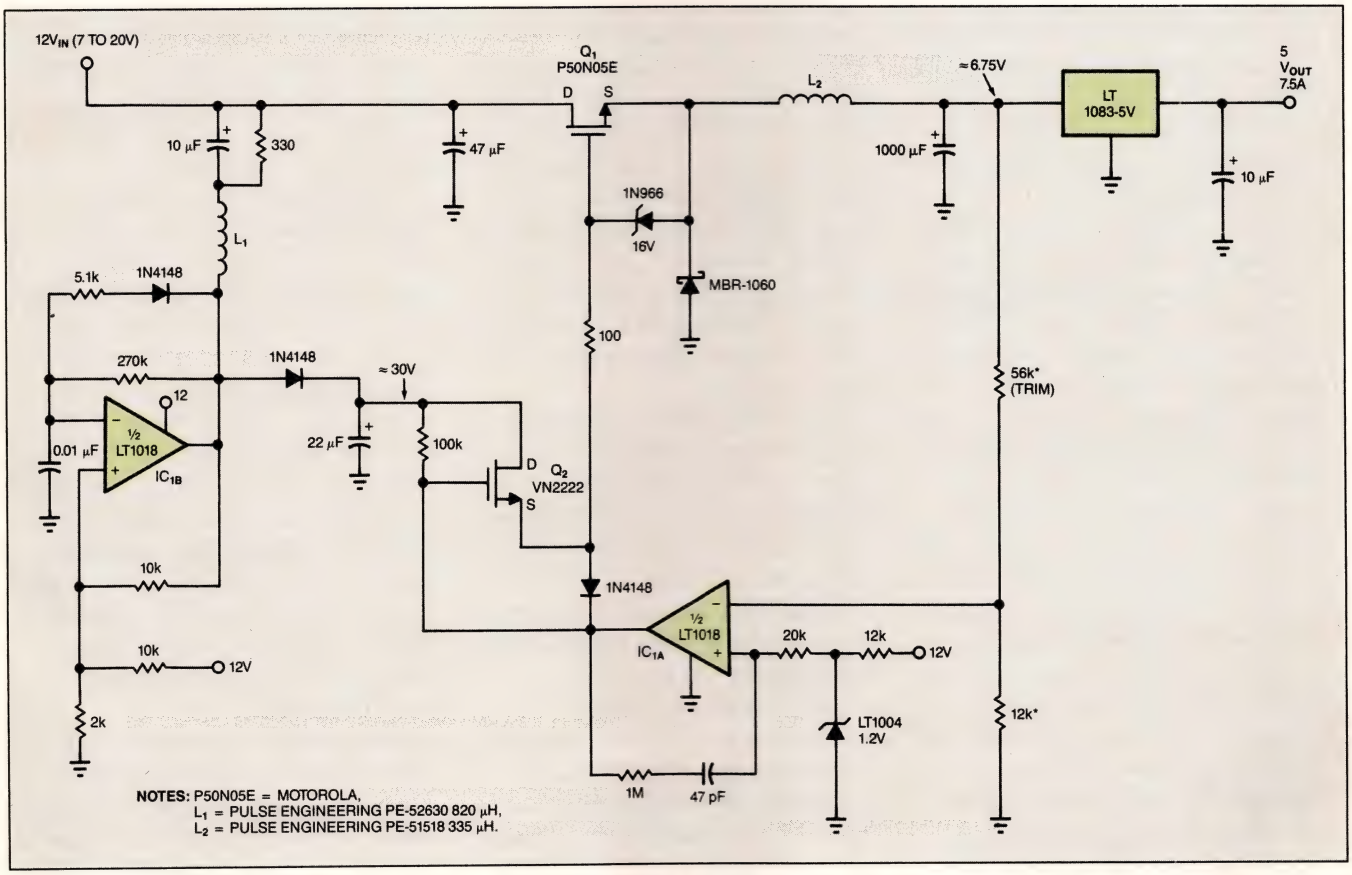


Fig 4—**Designed for low losses at high currents,** *this circuit is useful in applications involving dc inputs. The LT1083 functions normally; the remaining components form a switched-mode dissipation regulator.*

Wide voltage variations on the ac-line input have a deleterious effect on regulator efficiency.

the next half-cycle, the process repeats with the alternate SCR doing the work. The loop phase modulates the SCR's firing point to maintain a constant LT1086 input voltage.

The 1-μF capacitor around IC_1 compensates the loop, and the 10-kΩ resistor at IC_1's output ensures circuit startup. The 3-terminal regulator's current limit protects the circuit from overloads. This circuit has a dramatic impact on LT1086 efficiency versus ac-line swing. An important note here. The transformer in a preregulator can significantly influence the circuit's overall efficiency. One way to evaluate power consumption is to measure the actual power taken from the ac line.

Fig 4's circuit is useful when an application involves dc inputs—a regulated or unregulated power supply or a battery. This circuit features low losses at high current levels. The LT1083 functions in a conventional fashion, supplying a regulated output at 7.5A max. The remaining components form a switched-mode dissipation regulator, which maintains the LT1083 input level just above the dropout voltage under all conditions.

When the LT1083 input decays enough, IC_{1A}'s output goes high and increases the voltage on Q_1's gate. This rising voltage turns on Q_1, which drives current into L_2 and the 1000-μF capacitor and raises the input voltage at the LT1083 regulator. When the regulator input rises far enough, IC_{1A}'s output goes low, which turns

Achieving a low dropout voltage

Linear voltage regulators almost always use the design illustrated in **Fig A** for the basic regulating loop. The on-impedance limits of the pass element in the circuit establish the dropout voltage. The ideal pass element should have zero impedance between the input and the output and consume no drive energy.

Different pass elements offer different tradeoffs and advantages in establishing low dropout. Three are illustrated in **Fig B.** Emitter followers for transistors and source followers for MOSFETs offer current gain and easy loop compensation because the voltage gain is less than unity. They also transfer the drive current to the load. Unfortunately, you have to provide a voltage overdrive at the input to saturate a follower. Since V_{IN} must supply the drive, achieving overdrive is not an easy task. Practical regulator circuits must either generate the overdrive or obtain it from another source. You can easily generate overdrive in discrete regulator designs, but it's hard to do so with an IC power regulator.

Without voltage overdrive, the saturation loss is set by V_{BE} for bipolar transistors and by the channel on-resistance for MOSFETs. The on-resistance of a MOSFET varies considerably without overdrive, but bipolar losses are more predictable. Note that voltage losses in the drive stages add directly to the dropout voltage parameter. The follower output used in conventional 3-terminal IC regulators combines with the drive-stage loss to set the dropout at 3V.

Common-emitter configurations for transistors and common-source configurations for MOSFETs are another pass-element option. With bipolar devices, the common-emitter scheme removes the V_{BE} loss contribution. It's quite easy to saturate a pnp common-emitter driver, even in IC form. The tradeoff here is that the base current never gets to the load—a situation that wastes substantial power. At higher current levels, base drive current losses can negate a common emitter's saturation advantage. This is a particular problem in IC regulators, where the use of high-beta, high-current pnp transistors is not practical. At moderate current levels, pnp common-emitter drive stages are practical for IC-type regulators—the LT1020 and LT1120 use this approach.

Common-source, p-channel MOSFET configurations don't suffer from the drive-loss problems of bipolars but typically require 10V of gate-to-channel bias to fully saturate. In low-voltage applications, you have to generate negative potentials to satisfy the bias needs. P-channel devices also have poorer saturation characteristics than equivalent-size n-channel devices. The voltage gain available in common-emitter and common-source configurations creates some loop stability concerns, but these concerns are easy to handle.

Compound connections using a pnp-driven npn transistor are a reasonable pass-element compromise, particularly for IC-regulator devices with currents greater than 250 mA. With a compound

off Q_1 and terminates capacitor charging. The MBR-1060 damps L_2's flyback spike, and the 1-MΩ/47-pF combination sets loop hysteresis at about 100 mV.

Q_1, an n-channel MOSFET, has a saturation loss of only 0.028Ω but requires a 10V gate-to-source turn-on bias. IC_{1B} is set up as a simple flyback-voltage booster to provide about 30V of dc boost for Q_2. Q_2 serves as a high-voltage pullup for IC_{1A} to provide voltage overdrive to Q_1's gate. This overdrive ensures Q_1's saturation, even though Q_1 is configured as a source follower.

The 1N966 zener diode clamps excessive gate-source overdrives. These measures are necessary because there are no viable alternatives—low-loss, p-channel MOSFET devices aren't available, and bipolar approaches require excessive drive currents or have poor saturation characteristics.

Satisfy ultralow dropout needs

In some applications, extremely low dropout is a primary design target. The circuit in **Fig 5** is substantially more complex than a 3-terminal regulator design, but it features a 400-mV dropout level at an output of 10A. This circuit uses the same overdriven-source-follower technique employed in **Fig 4** to significantly lower saturation resistance.

The LT1072 switching regulator, set up as a flyback converter, generates Q_1's gate-boost voltage. This 30V boost voltage drives IC_{1A}. IC_{1A} compares the circuit

connection, the tradeoff between the pnp V_{CE} saturation term and the reduced drive losses compared with a straight pnp is favorable. Also, the major current flow is through a power npn—a configuration that's easy to achieve in monolithic form. The compound connection has voltage gain, so you have to pay attention to loop frequency compensation. LT1083-6 regulators use the compound connection for a pass scheme and employ a capacitor at the output to provide loop compensation.

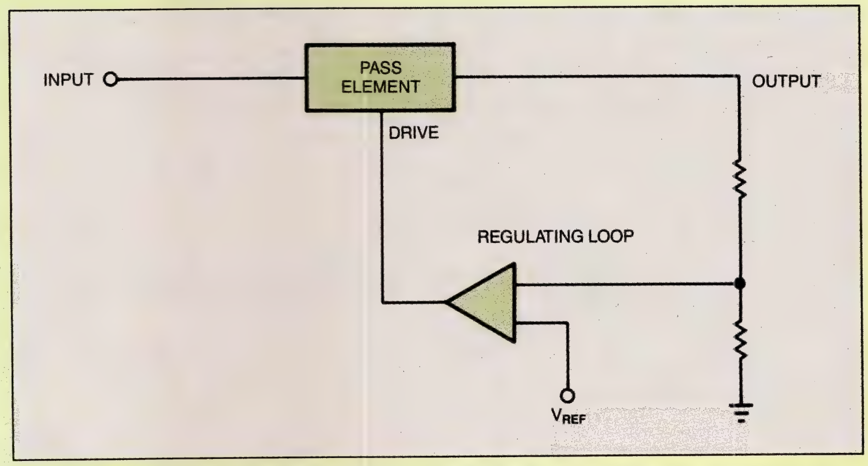


*Fig A—**Dropout-voltage limitations are controlled** by the pass elements used in this basic regulating loop, which is used in just about all linear regulators.*

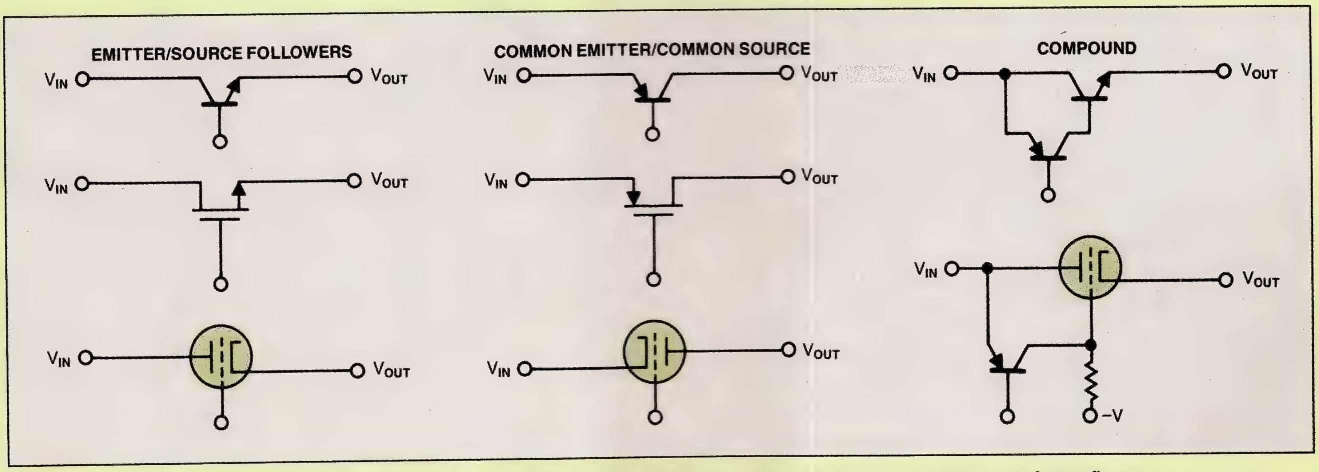


*Fig B—**These three pass elements** offer various tradeoffs and advantages in achieving low dropout-voltage figures.*

Power-type regulators can also benefit from low-dropout design techniques.

output to the LT1004 reference and servo controls Q_1's gate to close the loop.

The gate-voltage overdrive provides the low-dropout characteristic for this regualtor by enabling Q_1 to attain a 0.028Ω saturation level. The 1N966 zener diode clamps excessive gate-source voltage, and the 0.001-μF capacitor stabilizes the loop. IC_{1B} senses current across the 0.01Ω shunt to provide current limiting by forcing IC_{1A}'s inverting input to swing negatively. The low-resistance shunt limits loss to only 100 mV at 10A outputs. Circuit roll-off is smooth and evidences no oscillation or undesirable characteristics.

Fig 6 combines the best features of the previous designs to develop a regulator that features high efficiency at high power levels. This circuit combines **Fig 4's** preregulator techniques with the low-dropout design feature of **Fig 5.** There are, of course, some modifications.

For example, there is no boost supply for the linear regulator, and the 1N967A has a slightly higher zener voltage than the 1N966 in **Fig 5.** In addition, a single 1.2V reference serves the needs of both the preregulator and the linear-output regulator. The increase in zener-clamp values ensures adequate boost voltage lev-

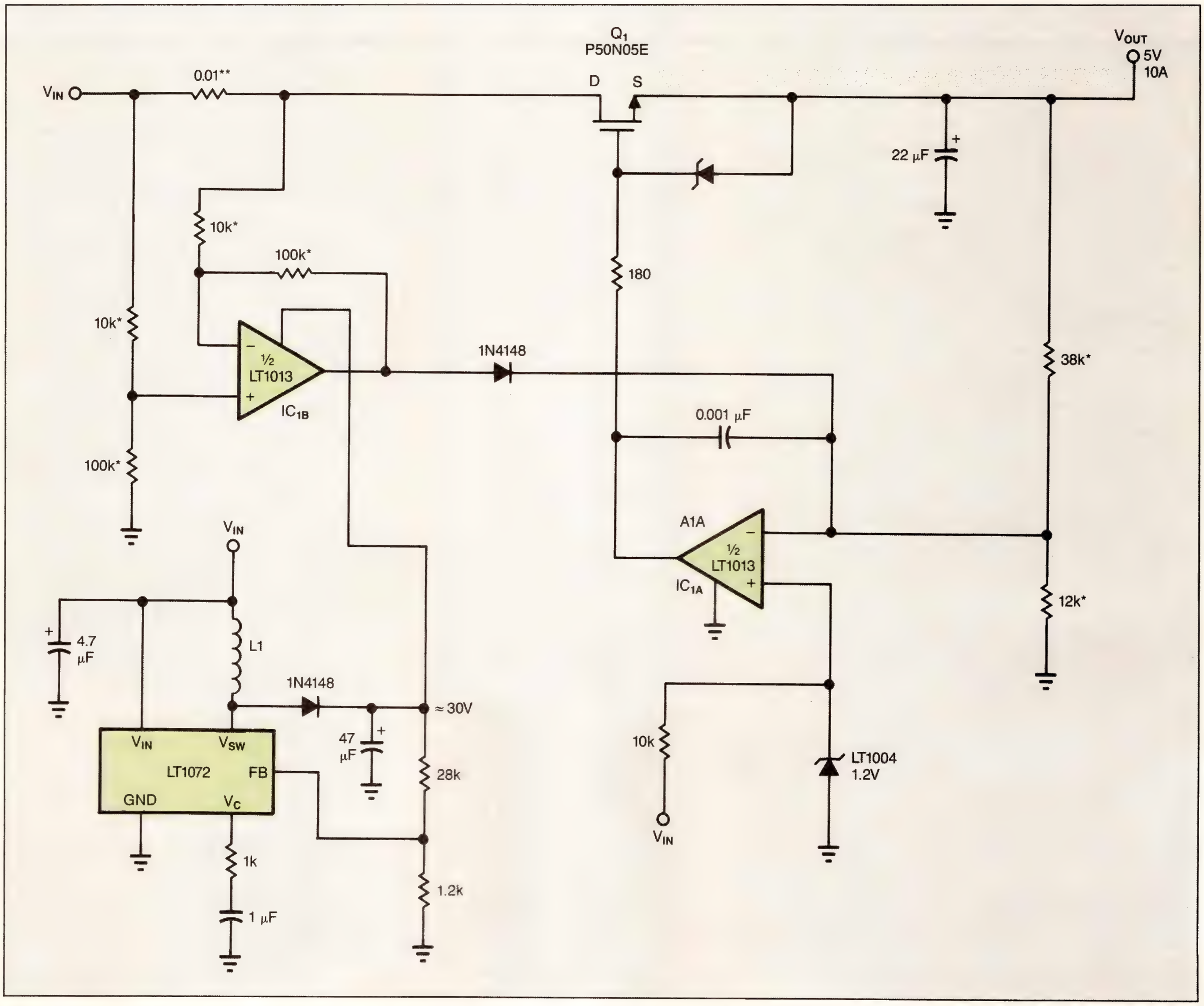
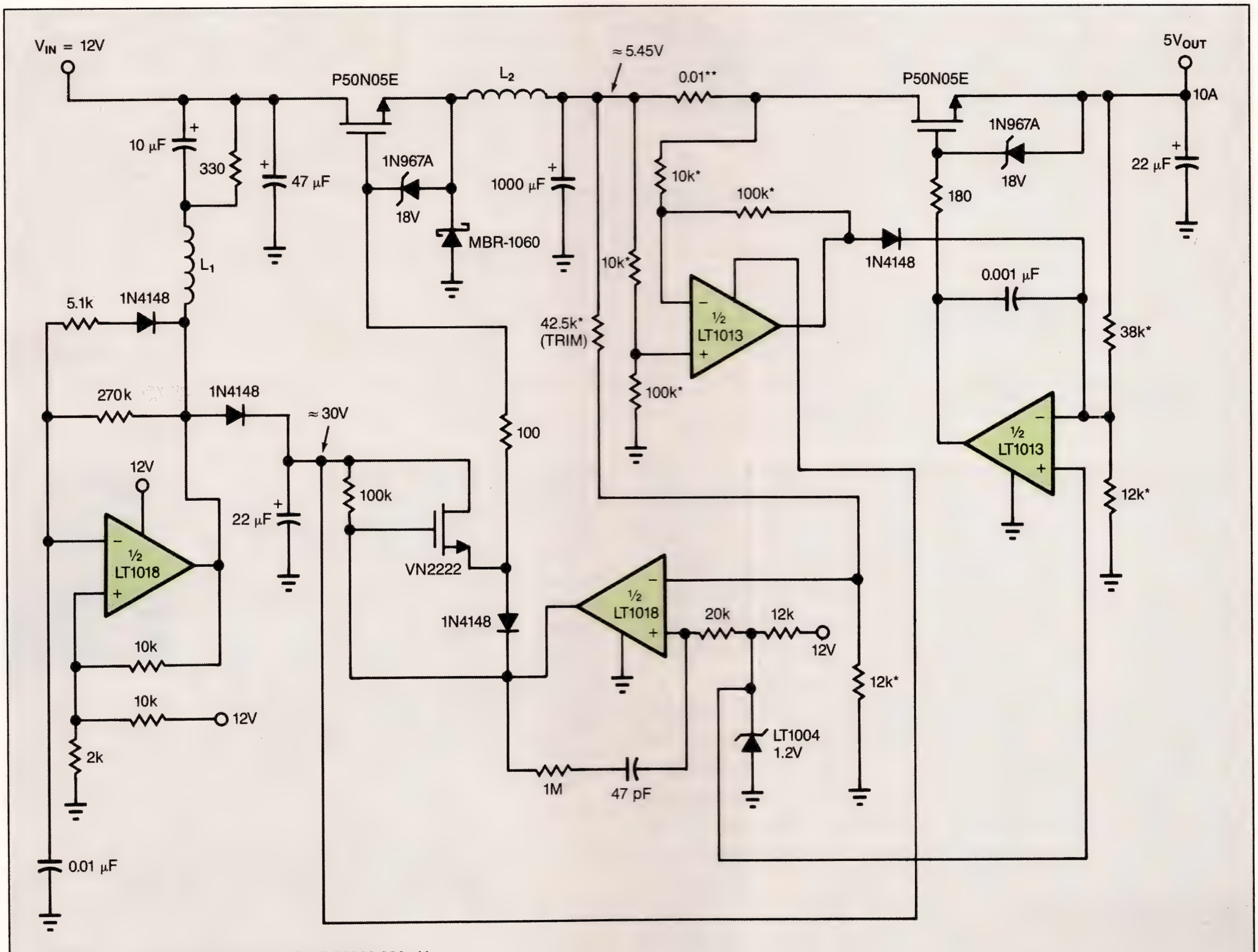


***Fig 5—Extremely low saturation resistance** is a key benefit provided by the source-follower techniques employed in this regulator. Although it's somewhat complex, the design features a 400-mV dropout voltage at 10A output levels.*

els for low-voltage input conditions. The preregulator's feedback resistors set the linear regulator's input voltage just above its 400-mV dropout level.

Although **Fig 6**'s circuit is complex, its performance is impressive. The circuit's efficiency is 86% at a 1A output level and decreases to 76% at full load. Circuit losses are essentially shared by the MOSFETs and the MBR1060 catch diode. You can improve efficiency by 3 to 5% by replacing the catch diode with a synchronously switched FET and trimming the linear regulator's input to the lowest possible dropout value.

Power linear regulators are not the only circuits that can benefit from the above techniques. **Fig 7**'s preregulated micropower linear regulator features excellent efficiency and low noise. A drop at the preregulator's output—pin 3 of the LT1020 regulator—causes the LT1020's comparator to go high. This transition switches the 74C04 inverter chain and biases the p-channel MOSFET on, thus allowing current to flow through the inductor. When the voltage at the junction of the inductor and the 220-μF capacitor gets high enough, the comparator output goes low and turns off the MOSFET's current flow. This loop action regulates the LT1020's input pin at a value established by the



NOTES: L_1 = PULSE ENGINEERING PE-52630 820 μH,
L_2 = PULSE ENGINEERING PE-51518 335 μH,
* = 1% FILM RESISTOR,
** = DALE RH-10.

Fig 6—To achieve highly efficient linear regulation, *this circuit combines a preregulator with a low-dropout regulator design. The circuit's efficiency is 86% for 1A outputs and 76% at full load.*

The on-impedance limitations of regulator pass elements determine dropout-voltage figures.

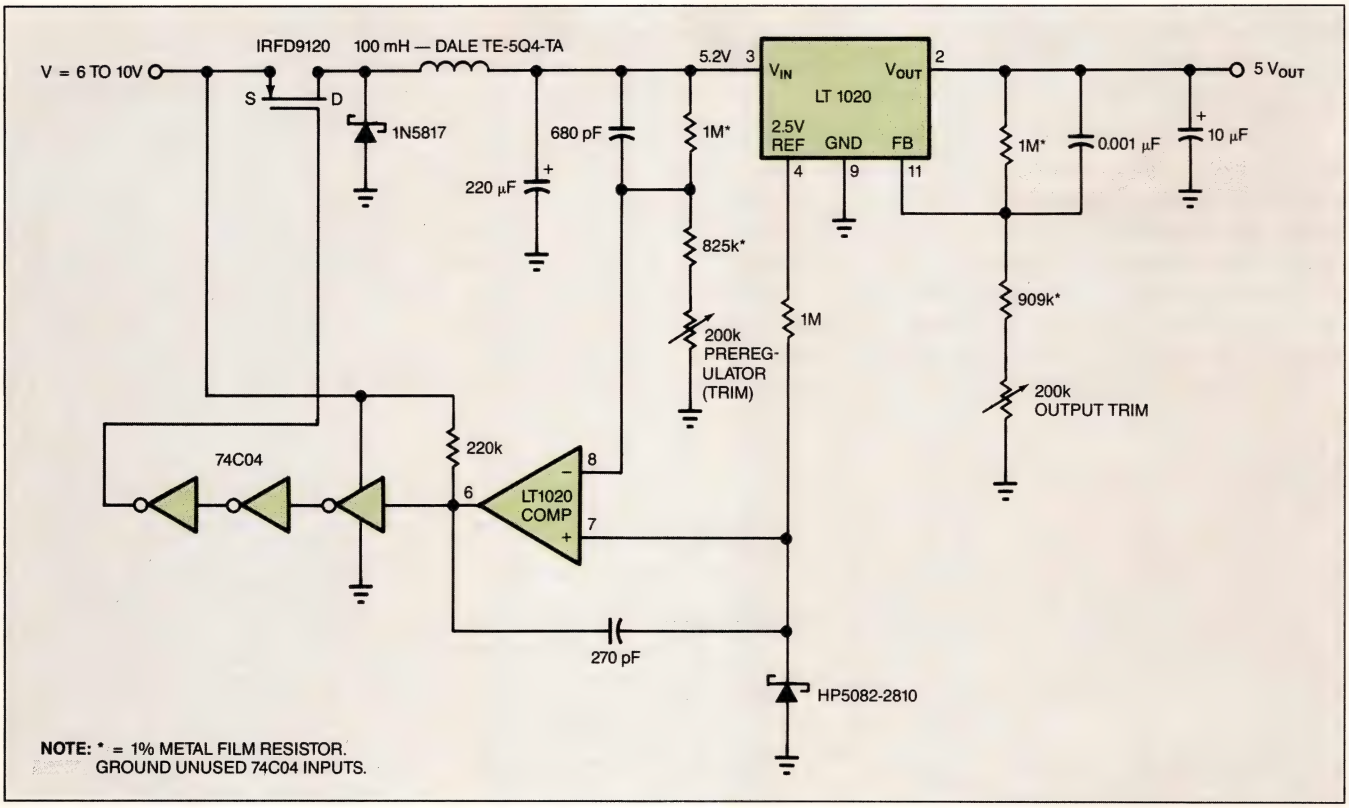
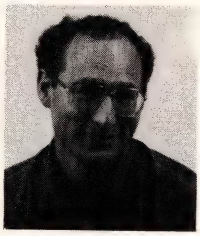


***Fig 7—High efficiency and low noise** are key features of this micropower regulator circuit. Despite its low, 40-μA quiescent current drain, the circuit can achieve efficiencies exceeding 80%.*

resistor divider at the comparator's inverting input and the LT1020's 2.5V reference. The 680-pF capacitor stabilizes the loop and the 1N5817 serves as a catch diode. The 270-pF capacitor facilitates comparator switching, and the HP5082-2810 diode prevents negative overdrives. The low-dropout LT1020 linear regulator smoothes the switched output signal. The output voltage is set by the resistive divider on pin 11.

Start-up poses a potential problem for this circuit. Although the preregulator supplies the input for the LT1020, the preregulator relies on the LT1020's internal comparator to function properly. As a result, the circuit requires a start-up mechanism. The 74C04 inverter chain provides one. When you apply power, the LT1020 sees no input but the inverters do. The 220-kΩ resistive path lifts the input of the first inverter high, thus causing the third inverter to turn on the MOSFET to start the circuit. The inverter's rail-to-rail swing also provides good MOSFET grid drive. The circuit in **Fig 7** has a quiescent current level of only 40 μA and achieves efficiencies in excess of 80% at output levels as high as 50 mA. **EDN**

Author's biography



Jim Williams, staff scientist at Linear Technology Corp (Milpitas, CA), specializes in analog-circuit and instrumentation design. He has served in similar capacities at National Semiconductor, Arthur D Little, and the Instrumentation Development Lab at the Massachusetts Institute of Technology. A former student of psychology at Wayne State University, Jim enjoys tennis, art, and collecting antique scientific instruments.

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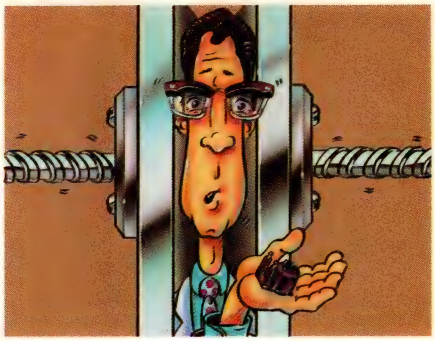
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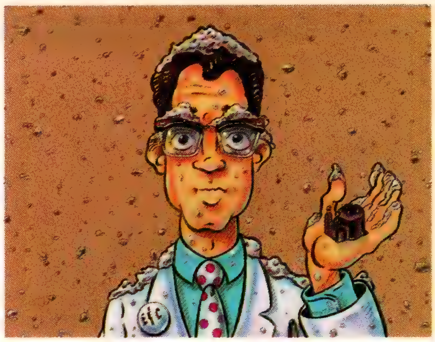
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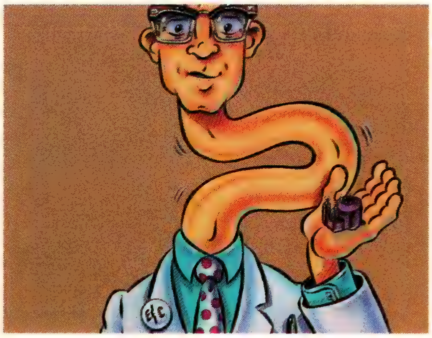
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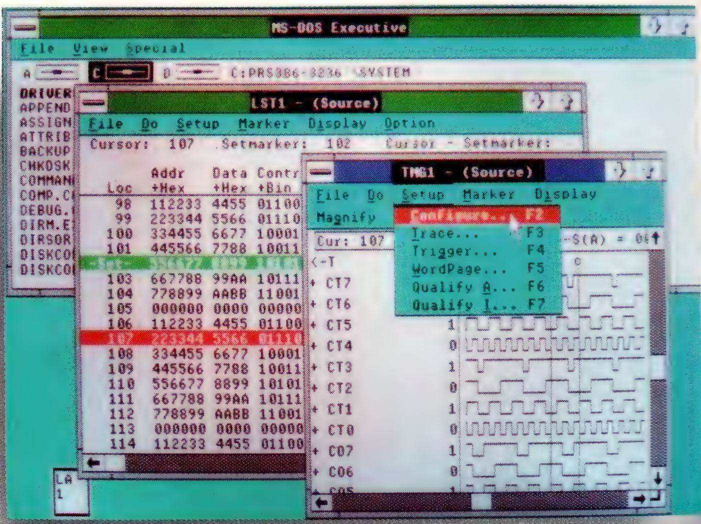

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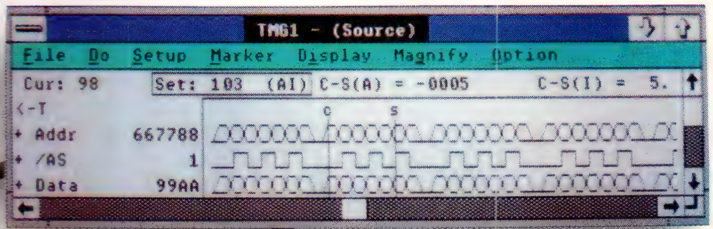

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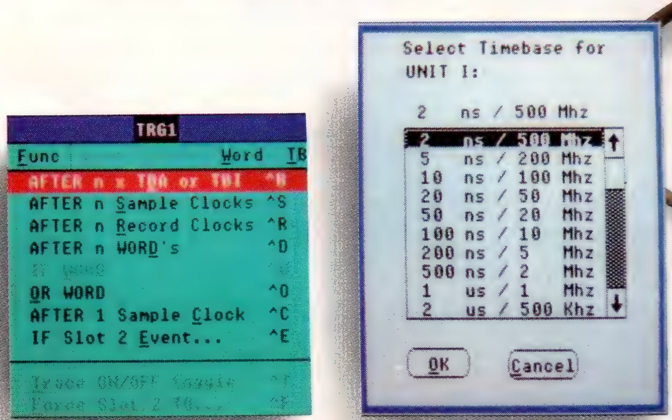

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Differential techniques move TDR into the mainstream

No longer the esoteric armament of the microwave world, time-domain reflectometry and time-domain transmission now meet a variety of today's troubleshooting needs. Differential and multichannel TDR/TDT give a complete picture of system and component characteristics.

Jon Lueker, *Tektronix Inc*

Improvements in TDR/TDT (time-domain reflectometry and time-domain transmission) allow you to quickly make vital component and system measurements that for a long time were difficult to accomplish. For example, you can now purchase instruments that perform differential and multichannel TDR and TDT. By using an oscilloscope that provides these capabilities, you can determine characteristics as diverse as the crosstalk and signal degradation in a ribbon cable, or the input, transmission, and common-mode rejection characteristics of a differential video amplifier.

Although the concepts underlying TDR/TDT technology aren't hard to grasp, if you fail to understand some subtleties—of how the instruments function and how to properly connect a unit under test—you are likely to experience frustration and obtain results of questionable validity.

Time-domain reflectometry is analogous to radar in that a signal is sent into a component and its reflection is detected; the characteristics of the reflection reveal the characteristics of the component. The signal sent into the component is usually a voltage step, and the shorter the step's rise time, the better. An oscilloscope displays the step's reflection. An equivalent-time sampling scope is now often used for TDR/TDT because, compared with a real-time scope, it can more easily provide the bandwidth and timing resolution needed to clearly resolve the most subtle signal features.

Older test setups often used separate pulse generators and oscilloscopes for TDR, but for reasons of performance and simplicity, the digital oscilloscopes used today for TDR usually incorporate a pulse generator. A TDR/scope combination (the name of the instrument is usually denoted by the same abbreviation as is used for the technique: "TDR" for time-domain reflectometer) can deliver high performance more easily because the manufacturer matches the scope and signal generator and specifies the system's overall response. The Tektronix 11800 digital sampling oscilloscope used in this article's application examples, for instance, provides a 35-psec max system rise time (reflected) when used with Tektronix's SD-24 TDR/sampling head. The step generator itself, though not directly specified, has a rise time typically less than 20 psec.

By comparison, TDR systems assembled from separate high-quality subsystems frequently achieve a much slower system rise time, often in the 500-psec to 5-nsec range. The slower response results in less information about the unit under test. This shortcoming becomes especially apparent when testing systems

Time-domain reflectometry is analogous to radar in that a signal is sent into a component and its reflection is detected.

that must deal with rise times shorter than 1 nsec (for example, ECL or GaAs logic systems).

By detecting the signal that passes through the component, rather than the signal's reflection from the component, you can use the same oscilloscope for TDT as well as TDR. Thus, TDT takes advantage of the same high-performance equipment used for TDR to determine such parameters as the gain of an amplifier, the attenuation of a pad, the loss of a ferrite bead, or the value of an inductor.

See the meaning in TDR traces

TDR and TDT display their results in the time domain. Specifically, the TDR traces you see on the oscilloscope show impedance variations as the step travels through the component under test. Because the time required for the step to go out from the scope and reflect back equates to distance, you can tell where impedance variations occur. For example, the first major reflection on a TDR trace might correspond to the point where the cable from the scope is soldered to a pc-board trace. This reflection is due to the mismatch between the impedance of the coaxial cable, which connects the scope to the board, and the impedance of the circuit trace being characterized.

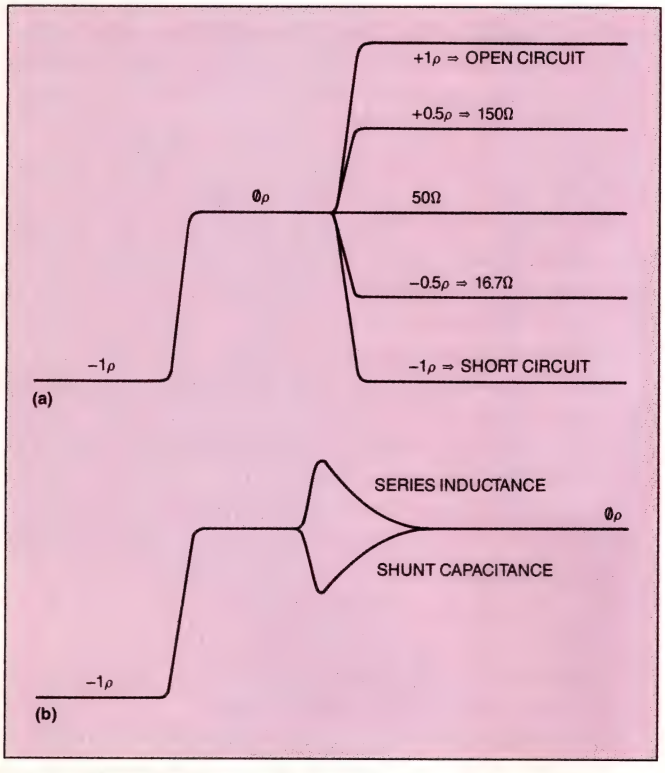

***Fig 1—Discontinuities in the impedance** of a transmission line show up as upward and downward steps **(a)** in a TDR display. Lumped inductance and capacitance **(b)** appear as decaying steps from whose time constants you can calculate the lumped-element values.*

The height of the reflection from the coax-to-pc-board transition shows the impedance of the pc-board trace. To understand what the height means, note that the reflection from an open circuit (such as an unterminated length of wire) appears as a positive step; the reflection has the same amplitude as the incident step (**Fig 1**). In contrast, a step reflected from a short circuit (a wire connected to ground) shows up as a negative reflection of the same amplitude as the incident step. Between these extremes, positive and negative voltage steps indicate differing impedance levels. The expression

$$2 \cdot \rho = (Z - Z_0)/(Z + Z_0)$$

predicts the reflection height (ρ) when a signal passes from a line of impedance Z_0 to a line of impedance Z.

A further bit of information you can get from a TDR trace is the inductance or capacitance associated with a component. Whereas rectangular features in the TDR trace indicate line-impedance changes, exponential features indicate a lumped inductance or capacitance. The time constant associated with the component produces the exponential shape, and you thereby have enough information to quickly calculate the inductance or capacitance.

The ability to determine specific impedance at any point in a circuit can be important in many applications. Perhaps more important, though, is the intuitive feel you get from seeing the TDR trace's variations. The trace shows any potential problem areas at a glance, in contrast to the hit-or-miss methods that are commonplace without TDR. In fact, when TDR is not available, problems with impedance mismatches can come to light only when a circuit does not work correctly. For example, an intermittent glitch on a TTL backplane caused by poor signal interconnection might take hours or even days to track down using traditional methods; TDR often reveals such problems in minutes.

You can get similar information about a system by using a network analyzer. These instruments are primarily useful for characterizing input and transmission parameters in the frequency domain, and they produce their results in the form of frequency-domain data. For most logic-design work, however, you think about problems in the time domain and you may conclude

that the convenience of differential and multichannel TDR removes many of the reasons for avoiding time-domain measurements when working with logic.

Single-ended TDR meets traditional needs

The simplest type of TDR has one single-ended channel. In this case, the TDR unit sends one step into one input of the unit under test and captures the reflections from that same input. This type of TDR has been used for many years for testing high-performance cables, connectors, and pc boards. TDR was used mainly for characterizing the latter two component types for RF and microwave work. TDR cable testing generally involves communication lines spanning longer distances, from yards to miles. During both installation and maintenance, cables are checked with TDR to ensure that the cable, with its splices and taps, passes signals cleanly.

Single-ended TDR/TDT has found a growing number of applications as digital systems get faster. However, many high-speed signals that must propagate for any significant distance (even just a few inches at high frequencies) are transmitted differentially to preserve signal quality. Obtaining valid differential results with a single-ended TDR system is difficult in many cases—and is occasionally impossible. In general, simple addition of single-ended TDR values does not give differential results; if you use single-ended TDR in a differential system, you must be careful to properly apply Thevenin's theorem when converting from differential to single-ended configurations. Furthermore, you must usually make at least two single-ended measurements to obtain the data you could obtain from one differential measurement. Single-ended TDR/TDT thus can have frustrating limitations for digital designers, who are increasingly using such structures as twisted pairs, ribbon cables, and coupled lines to transmit their critical differential signals, and who are often under intense time constraints.

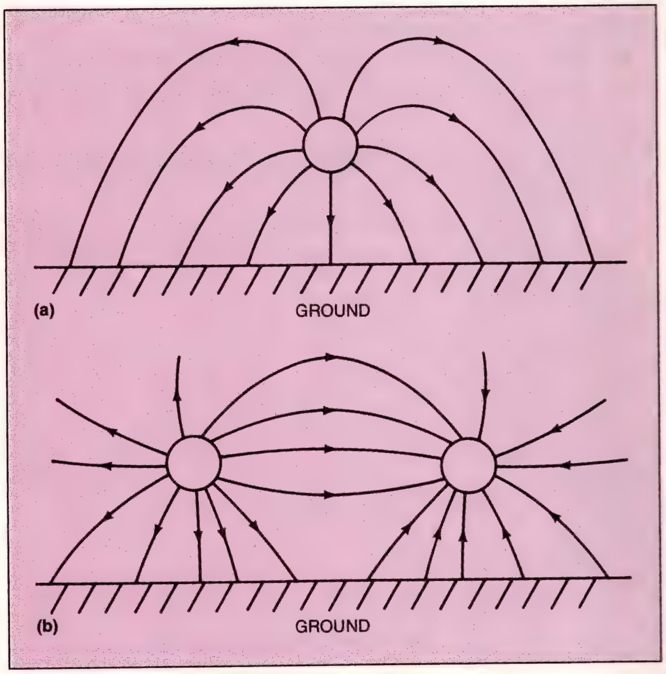

*Fig 2—**The electric fields** surrounding a conductor carrying a single-ended signal **(a)** are much diffferent from those in the vicinity of a pair of conductors **(b)** carrying a differential signal. The differences help to explain why you must use care in applying single-ended TDR to differential systems.*

The explanation of the complexity of obtaining differential results with single-ended TDR calls forth some involved transmission-line theory. You can quickly grasp the underlying reasons, however, by examining the nature of a differential line (**Fig 2**). Such lines usually have a ground structure and two signal conductors, which carry differential (complementary) signals. The fields generated by the complementary signals tend to couple the signal lines directly, rather than simply coupling each line independently to ground. Differential lines have two great advantages. First, at a distance from the lines, fields tend to cancel out, leaving very little radiated EMI or RFI that could cause problems elsewhere (in the form of crosstalk, for example). Further, the differential signals tend to shrug off external noise because each line senses the noise equally; this common-mode noise is not detected by the differential receiver, which senses only the difference between the complementary signals.

The reason why single-ended TDR can fail to work with differential lines lies in the interaction between the complementary conductors. If you only excite one of these conductors, the transmission effects differ greatly from those you see when both conductors are interacting differentially. If a twisted pair suspended over a ground plane is excited differentially with steps at $\pm V$, only the differential mode of propagation is excited and then measured. You can think of a single-ended TDR pulse of amplitude $+V$ driving only half of the pair as the sum of the differential excitation of $\pm V/2$ and a common-mode excitation of $+V/2$ (on both conductors). This combination simultaneously creates differential and common-mode signals, which can have different impedances and propagation velocities. The resulting display on the instrument screen can be a

The same oscilloscope used for TDR can be used for TDT by detecting the signal that passes through the component rather than the signal's reflection from the component.

complex waveform that masks the useful information. If you are working with differential lines, you'll probably find that differential TDR/TDT makes your life a lot easier.

Differential TDR/TDT is really a special case of multichannel TDR/TDT in that a differential test requires step generation and signal acquisition on two channels. Each channel must have the flexibility to generate a step in the positive or negative direction so that you can set up the necessary complementary signals for differential testing. By using positive-going or negative-going steps on both differential channels, you can also check a differential component's response to common-mode signals.

Moreover, there are benefits to having four or even more TDR/TDT channels. With four channels, for instance, you can simultaneously perform differential TDR and TDT, or perform differential TDR while checking for crosstalk on another differential line.

More than four TDR/TDT channels can prove invaluable for automatic test equipment (ATE) use. In a high-speed chip tester, for instance, a large number of TDR channels assists in deskewing signal lines precisely—an operation that high-throughput TDR handles in seconds, compared with the hours of work cable characterization can require.

Two typical application examples, with tips for obtaining good results, illustrate the usefulness of differential and multichannel TDR/TDT. In these examples, TDR/TDT sheds light on design factors that have long plagued digital circuits. Crosstalk, for example, has long been difficult to predict and control. You generally discovered crosstalk only when your circuit began to fail intermittently. And even then you could only guess that crosstalk was the culprit. Multichannel TDR/TDT provides a quick way to quantify crosstalk and other potential problems.

The first application example involves a 2m-long, 20-conductor ribbon cable that connects two synchronous digital circuit boards. The cable carries eight bits of bidirectional data plus a clock and a data signal generated by one of the boards. (Though use of such a long ribbon cable to carry high-speed digital signals is an example of a questionable design practice, it represents a situation that occurs all too frequently.) A wire mesh covers one side of the cable for ground purposes; pin 1 connects to this ground mesh. The cable manufacturer may furnish performance specs for the bare cable, but when you add connectors, the cable's characteristics can change dramatically.

The clock is the most critical signal carried by the cable because any variations in the clock waveform can mean that data is not strobed into latches correctly. (Setup and hold times for the data and direction signals prevent problems on those lines.) For a high-speed TTL or ECL system, there are several potential design problems you must investigate:

- Will the ribbon cable pass the clock without rounding off the corner of its rising edge too much?
- Will reflections in the ribbon cable disrupt the clock?
- Will crosstalk cause problems under some circumstances?

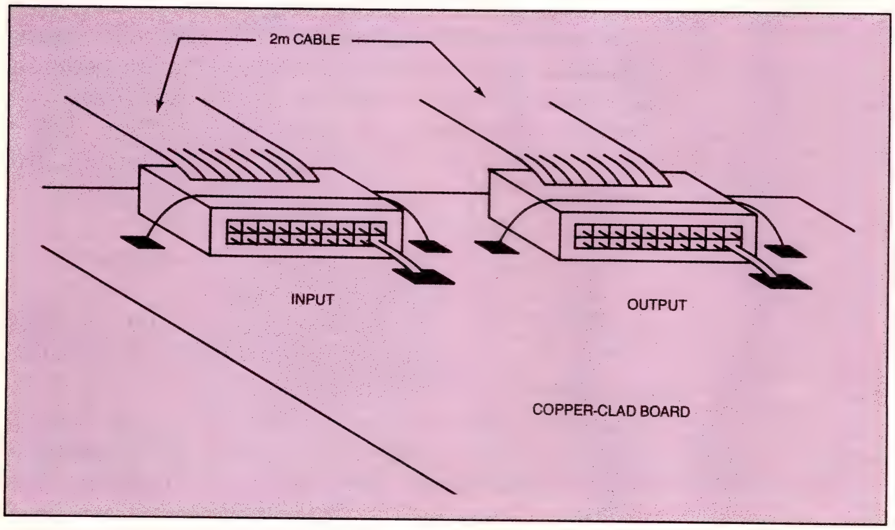

***Fig 3—When you apply TDR** to a ribbon cable, you need to make sure that the ground connections between the cable and your pc board are as short as you can make them. This same rule applies to the signal and ground connections between the cable connectors and the TDR instrument.*

- Should you use a differential line for the clock to ensure correct operation?

If you have answered one or more of these questions in the affirmative, you would be wise to make all the measurements differentially.

A simple setup plumbs a ribbon cable

An easy way to make these measurements is to fasten the connectors on both ends of the cable to a piece of copper-clad board (**Fig 3**). You can do so with glue or by soldering a wire across each connector, orienting the connectors so that the pins are parallel to the board. Insert a pin into socket 1 of each connector and solder the pins to the board. Be sure to keep these ground pins as short as possible.

This simple arrangement allows you to make all the necessary measurements in an environment that simulates an actual board-to-board connection. For convenience, one connector on the cable shown in **Fig 3** is labeled as the input and the other connector as the output. You insert TDR pulses into the input connector; you monitor TDT results at the output connector.

You can make connections from the scope to the ribbon cable using 50Ω coaxial cable with a pin soldered to the cable's center conductor. Gather the coax's ground braid to one side and leave it dangling. You can now insert the pin into any of the connector's sockets and tack solder the coax's ground braid to the board. It is crucial to keep both the signal pin and ground connection from the coax as short as possible—no longer than about 0.2 in. If possible, the coax should touch the connector when you insert the pin. When you move the coax from socket to socket, move the ground braid too, so that you always minimize the length of the ground connection.

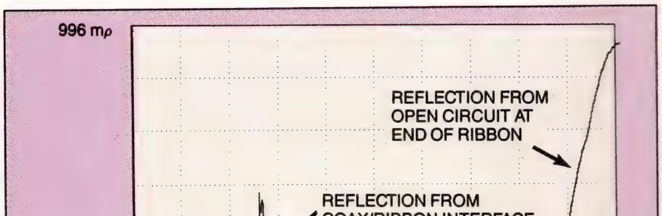

*Fig 4—**If the impedance of a pc-board trace** is slightly greater than that of a coaxial cable that brings a signal to the board, the TDR display will show a small positive step. The large step at the far right is the result of an open circuit at the end of the pc-board trace, and the "pulse" that precedes the small step is the result of an impedance discontinuity where the cable joins the board.*

To perform single-ended TDR on wire 2 of the ribbon cable, insert the coax pin and tack down the braid. Then run the scope's procedure for TDR. In the Tektronix 11800 scope, pop-up menus lead you through the set-up procedure and allow you to display results in terms of either millivolts or the reflection coefficient, ρ. The latter is the traditional unit for TDR and is based on the amplitude of the TDR step pulse. The amplitude of the step itself equals 1ρ, with all other amplitudes normalized to this value. Because ρ bears a mathematical relationship to impedance, you can use it in determining the impedance of a network at any point. The relationship for impedance is

$$Z = Z_0((1+\rho)/(1-\rho)),$$

where Z_0 is the characteristic impedance of the system. For the set-up described here, Z_0 equals 50Ω.

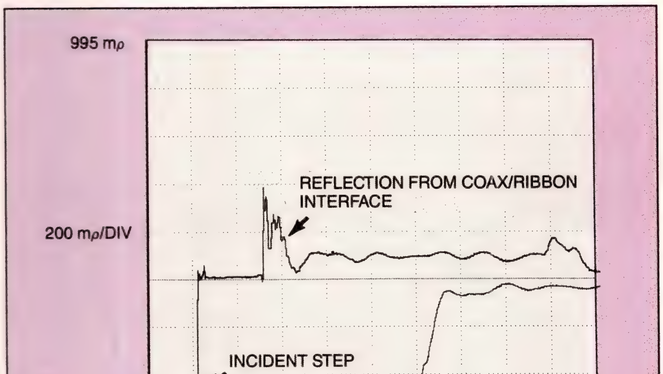

*Fig 5—**A TDT trace** superimposed on a TDR display shows how passing a step through a cable modifies the step.*

Because the time required for the step to go out from the scope and reflect back equates to distance, you can tell where impedance variations occur.

The TDR trace from the ribbon cable (**Fig 4**) shows the incident step leaving the sampling head (the first rise), entering the connector (the jumbled-looking part of the trace), and reflecting from the ribbon cable's open end (the second rise). You can determine precisely where the step enters the connector by using a screwdriver to short the wire at this point; the TDR trace will show a negative step at the short. With this reference point established, you can measure the precise electrical length of the cable. The time between this reference point and the positive reflection from the cable represents the "down-and-back" time of the cable itself. The electrical length of the cable is thus one half of that time.

Because the part of the TDR trace representing the step's passage through the ribbon cable is higher in amplitude than zero ρ, you can tell immediately that the ribbon cable's impedance is somewhat higher than 50Ω. Using the formula given above, the ribbon cable's impedance is

$$Z=50\Omega((1+\rho)/(1-\rho))=50\Omega((1+0.0833)/(1-0.0833))=59.12\Omega.$$

You can also detect the lumped inductance introduced by the connector. The short exponential and subsequent ringing at the coax/ribbon interface represent the inductance of the ground return due to the fact that all the ground currents must converge on pin 1 of the connector. This shared ground will also prove to be the most serious source of crosstalk.

Knowing the ribbon cable's exact impedance shows you the load your circuitry must drive. The cable's impedance also establishes the termination resistance you must use to match the cable, and thus minimize electrical reflections.

To see how the cable affects a step passing through it, you can use TDT (**Fig 5**). With a multichannel scope like the 11800, you use one TDR channel to insert a step and another channel in acquisition mode to detect the pulse when it emerges from the ribbon cable's output. Using a second channel of matched characteristics for receiving the TDT signal ensures that the system is well matched. Note that you can simultaneously execute the TDR and the TDT tests—which is also what you do on separate wires to perform the crosstalk test. Specifically, you insert a TDR step in one wire and use TDT to detect the signal induced on another wire.

To get a complete picture of the ribbon cable's crosstalk, you must determine the contribution of each wire in the cable. If, for example, you use wire 2 for your clock line because it is nearest the ground pin, you can expect wire 3 to contribute the most crosstalk, with other wires contributing less as the distance from

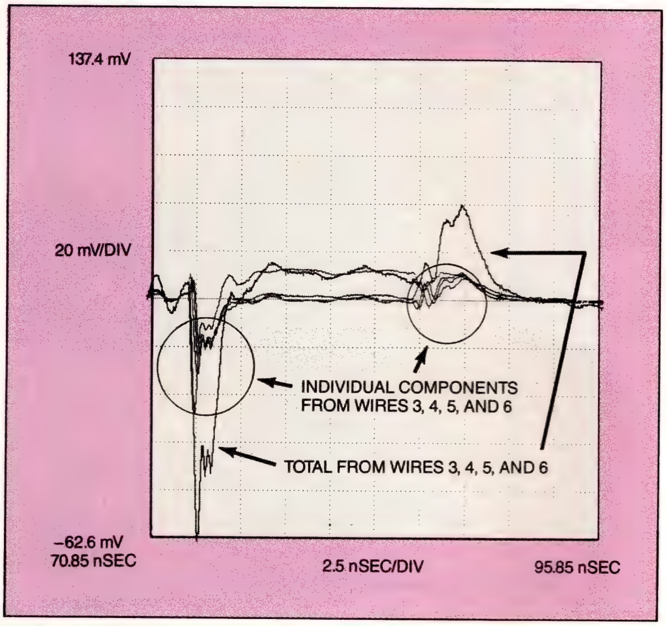

***Fig 6—Using multichannel TDR** and the scope's ability to add waveforms, you can observe how crosstalk from several signal lines affects a sensitive signal line.*

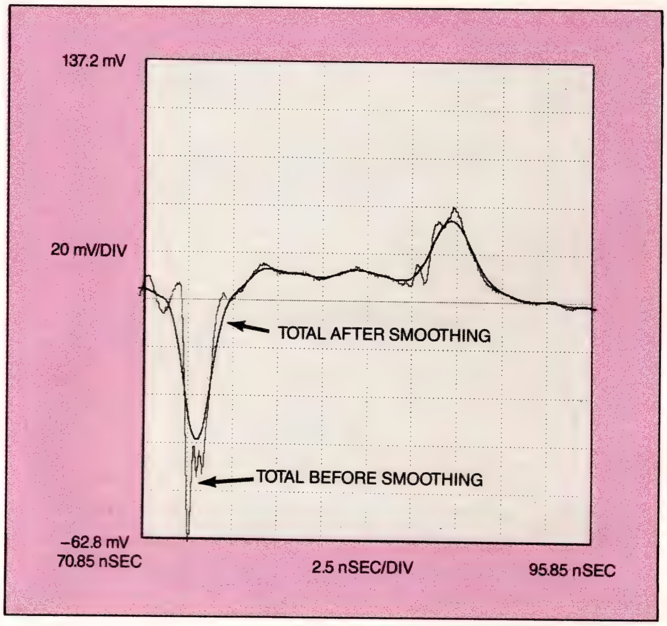

***Fig 7—The scope's lowpass filtering** or smoothing capability makes it possible to observe crosstalk effects only in the range of rise times that are significant to the logic family you are using.*

wire 2 increases. The rule of superposition says that you can add such electromagnetic contributions arithmetically to determine the total signal, as long as you maintain representative source and receiver impedances at the cable's ends.

To check crosstalk on the clock line, you can therefore put a step pulse into each data wire in turn, while measuring any signal coupled to wire 2. The digital sampling scope can record each TDT waveform and automatically sum them, presenting you with a picture of worst-case crosstalk. The results appear in **Fig 6**.

The crosstalk shown in **Fig 6** is induced by an extremely fast pulse. Even GaAs logic is unable to equal this pulse's 15-psec rise time. Slower signals will induce less crosstalk, but you need to determine how much less. To do so, you use the sampling scope's filtering feature to slow the TDR system rise time to show only results that are relevant to the logic speeds you are using.

For example, if you're using high-speed TTL, you might wish to use a TDR system with a 2-nsec rise time to approximate the actual signals in your system. If the scope contains a bandwidth-limiting filter, you will be able to select the scope's rise time and directly characterize structures with relevant signals.

Fig 7 shows the total crosstalk, again with filtering applied, and indicates that crosstalk is still a problem even at TTL speeds. Note that even after filtering to logic speeds, there is a peak in the crosstalk signal of roughly 25% of the voltage swings on the driven channels, a clear violation of system noise-margin requirements.

The amount of crosstalk on the clock wire makes it clear that a differential clock line is a wise choice. To make sure that a differential line will be adequate, you can check wires 2 and 3 differentially for crosstalk. **Fig 8** shows the crosstalk test again, except now you measure the induced signal on lines 2 and 3 differentially. Note the dramatic reduction after smoothing: The peak crosstalk is only 4% of the total voltage swing on the driven lines.

Another application example involves an active device—a differential linear amplifier. The specific device used in this example is a 10H116 ECL line receiver, which can be used as a linear RF amplifier at low signal levels, despite its logic-device label (**Fig 9**). The measurements described for this chip are useful for any high-speed differential amplifier.

The first test is to use differential TDR to determine the amplifier's differential input capacitance. To do this, you apply complementary input steps to the two inputs and examine the time constant of the reflected signal. (The SD-24 TDR/sampling head offers adjustable step amplitude, which permits a measurement within the linear input range of the 10H116.) Note that by using true differential TDR, you measure the

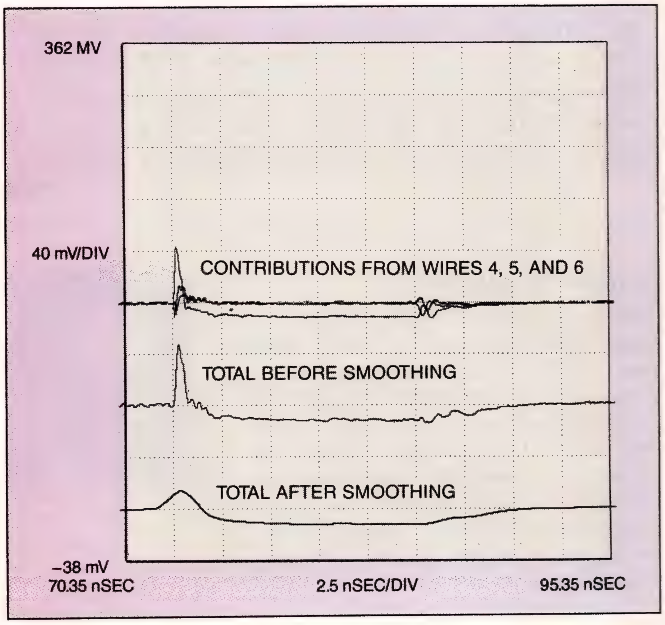

Fig 8—Using the ribbon cable's conductors *as differential pairs greatly reduces the crosstalk, as these differential TDR traces readily show.*

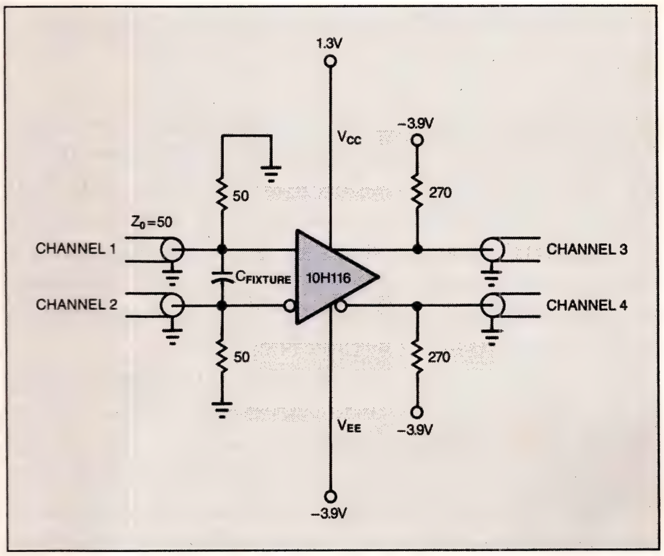

Fig 9—The setup for measuring *the common-mode rejection of this differential ECL line receiver is straightforward—at least at the schematic level.*

The time constant associated with the component produces the exponential shape, and gives you enough information to quickly calculate the capacitance or inductance.

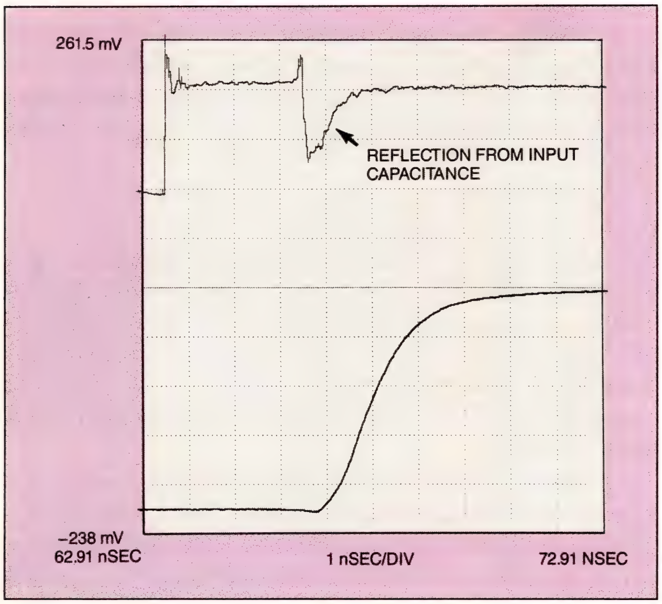

***Fig 10—Applying a 20-mV differential step** to the 10H116's input, as seen in the upper TDR trace at 10 mV/div, produces a differential output of approximately 200 mV, as seen in the lower TDT trace at 50 mV/div. In other words, the line receiver's gain is approximately 10. The lower trace also reveals a rise time of about 2.1 nsec.*

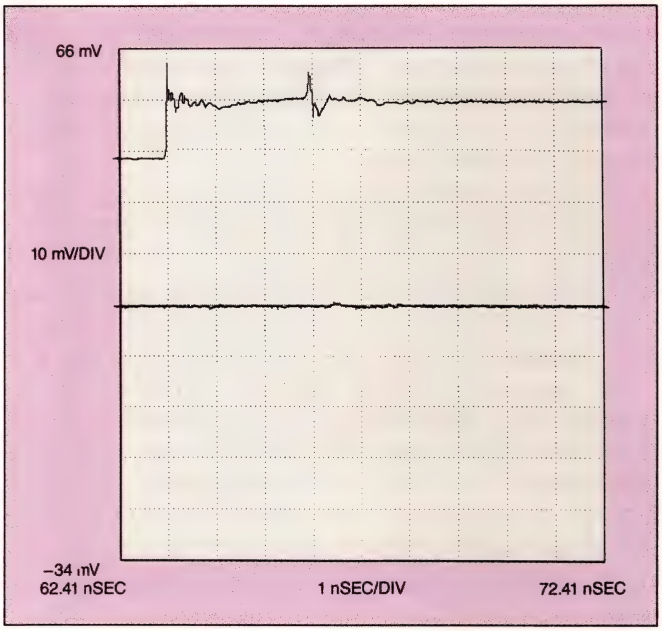

***Fig 11—Stimulating the 10H116** with a purely common-mode step (upper trace) produces very little output (lower trace), an indication of excellent common-mode rejection at all frequencies of interest.*

actual differential input capacitance of the chip; this value is somewhat higher than the combination of the two separate input capacitances measured with a single-ended TDR. As shown in **Fig 10**, the time constant is 400 psec, so

$$C = \text{Time}/R = 400 \text{ psec}/50\Omega = 8 \text{ pF (including test socket).}$$

The second test, the characterization of the chip's output response, follows easily from the first. If you are already applying a differential input that falls within the 10H116's linear region and your scope has an additional pair of acquisition channels, you can use them to examine the differential step at the chip's output. As you can see in **Fig 10**, the differential gain is roughly 10, and the rise time is 2.1 nsec.

One more test you can perform on the line receiver is to check how well it rejects common-mode noise. You do this by presenting the chip with a pair of step pulses of the same orientation, rather than the complementary pulses used in differential signals. Any corresponding signal on the chip's outputs indicates the device's susceptibility to common-mode noise. **Fig 11** indicates that the 10H116 has an excellent common-mode rejection ratio, even when driven with very high-speed common-mode inputs.

Many engineers will agree that before the advent of differential and multichannel TDR/TDT, some of the tests described here were impractical or even impossible. For example, a single-ended crosstalk test requires that you apply pulses and monitor signals at different points, something you can't do with a single-ended, single-channel TDR. As logic speeds continue to increase, differential TDR/TDT techniques are likely to become a requirement for large numbers of designers.

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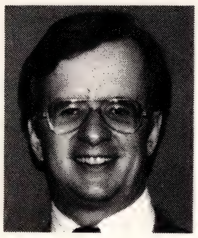
Author's biography



Jonathan Lueker is project leader for high-frequency sampling head development at Tektronix Laboratory Instruments Div in Beaverton, OR. He has been employed at Tek for over 7 years, and among the products for whose development he has been responsible is the SD-24 sampling head. Jon holds a BSEE from MIT. In his spare time, he enjoys traveling, skiing, bicycling, and carpentry.

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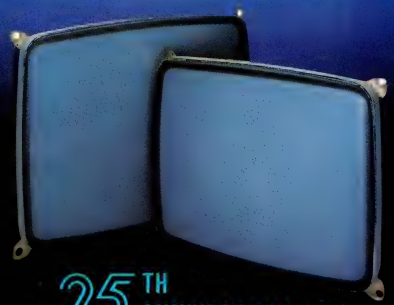

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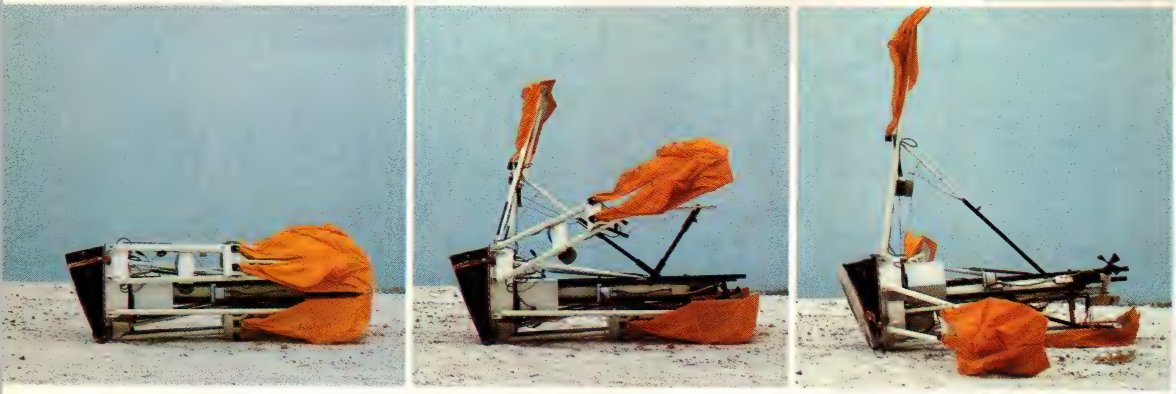

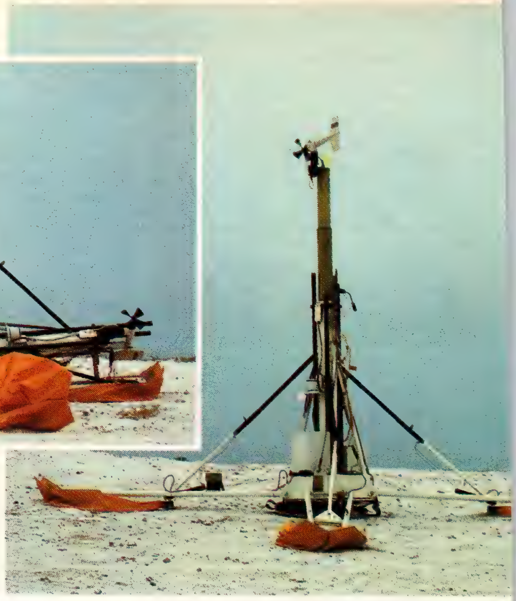

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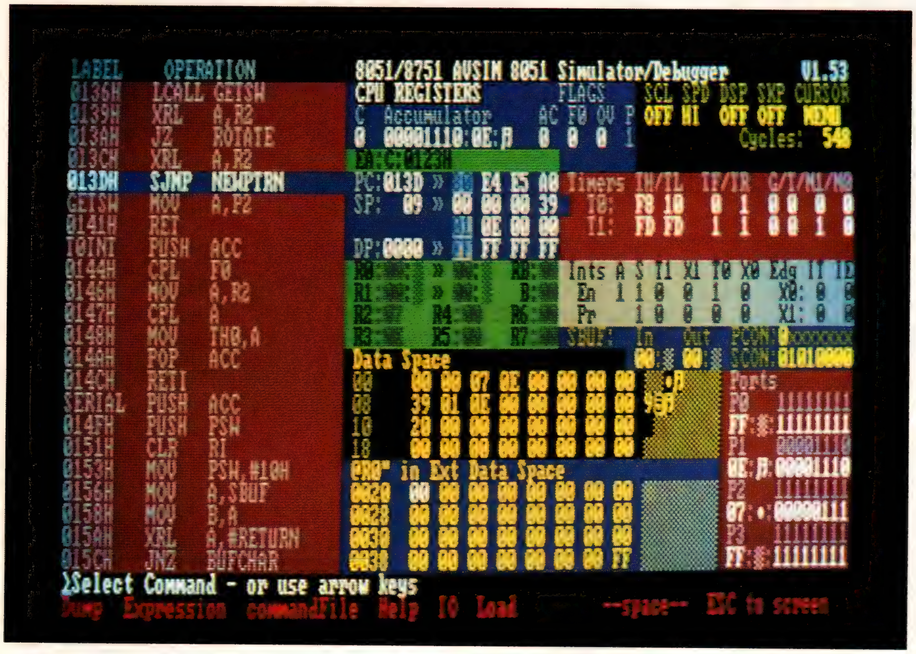

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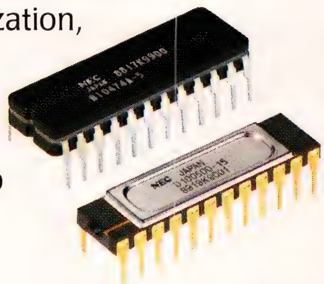

Device	Interface	Organization	Access time (ns)	Power consumption (W)	Supply voltage (V)	Package
µPB10422D-7/-10		256 x 4	7/10			24-pin ceramic DIP
B10470D-10/-15		4K x 1	10/15			18-pin ceramic DIP
B10474AD-5/-6		1K x 4	5/6			24-pin ceramic DIP
B10474D-8/-10/-15			8/10/15			24-pin ceramic DIP
B10480D-10/-15	ECL 10K	16K x 1	10/15	1.2	−5.2±5%	20-pin ceramic DIP
B10480B-10/-15						20-pin ceramic flat
B10484D-10/-15		4K x 4	10/15			28-pin ceramic DIP
B10484B-10/-15						28-pin ceramic flat
D10500D-15/-18		256K x 1	15/18			24-pin ceramic DIP
B100422D-7/-10		256 x 4	7/10			24-pin ceramic DIP
B100422B-7/-10						24-pin ceramic flat
B100470D-10/-15		4K x 1	10/15			18-pin ceramic DIP
B100474AD-5/-6			5/6	1.0		24-pin ceramic DIP
B100474AB-5/-6						24-pin ceramic flat
B100474D-8/-10/-15			8/10/15			24-pin ceramic DIP
B100474B-8/-10/-15		1K x 4				24-pin ceramic flat
B100474B-45/-50/-60	ECL 100K		4.5/5.0/6.0	2.0	−4.5±5%	
B100474K-45/-50/-60						24-pin LCC
B100480D-10/-15		16K x 1	10/15			28-pin ceramic DIP
B100480B-10/-15						28-pin ceramic flat
B100484D-10/-15				1.0		28-pin ceramic DIP
B100484B-10/-15		4K x 4	10/15			28-pin ceramic flat
B100484K-10/-15						28-pin LCC
D100500D-15/-18		256K x 1	15/18			24-pin ceramic DIP

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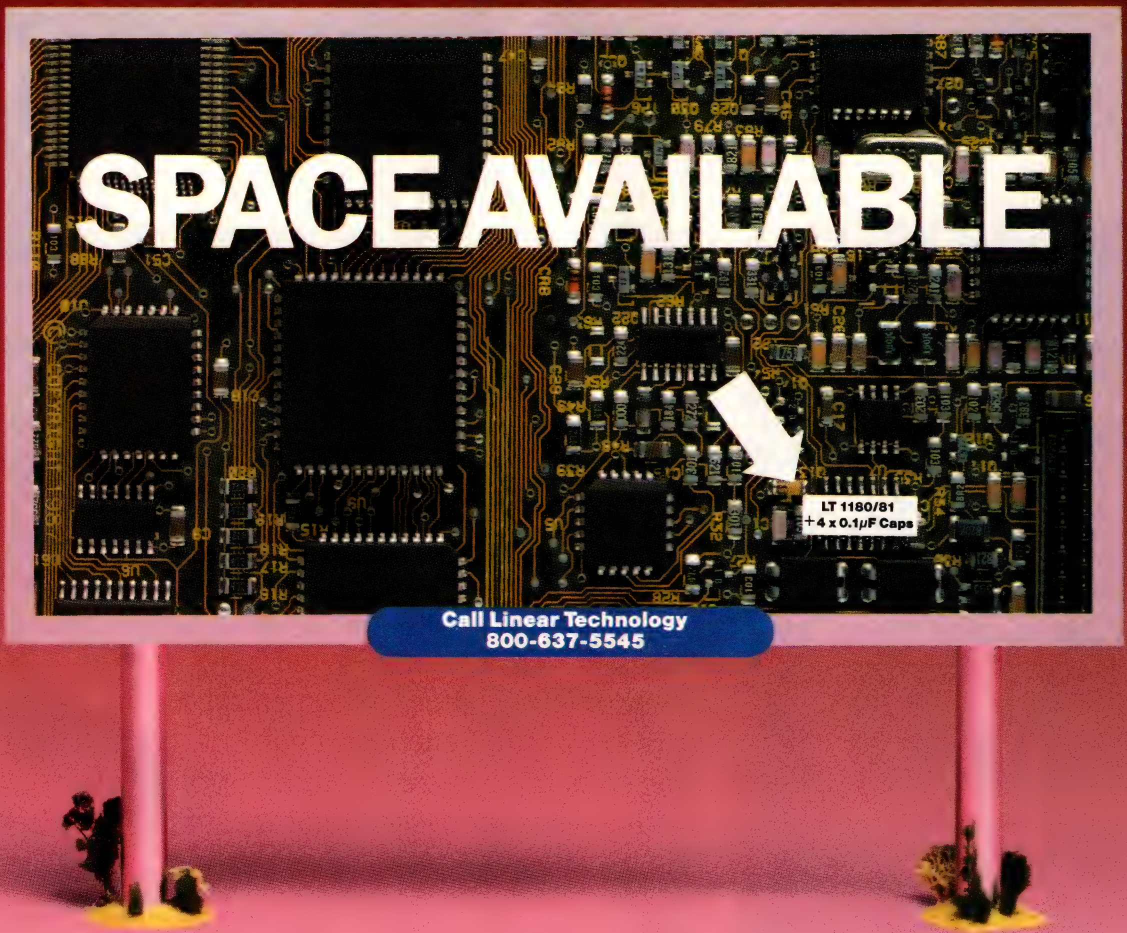

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LT1032	4	0	±12V	YES*	YES	N/A
LT1039	3	3	+5V, ±12V	YES*	YES	N/A
LT1039-16	3	3	+5V, ±12V	NO	YES	N/A
LT1080	2	2	+5V	YES*	YES	1μF
LT1081	2	2	+5V	NO	YES	1μF
LT1130	5	5	+5V	NO	YES	1μF
LT1131	5	4	+5V	YES*	YES	1μF
LT1132	5	3	+5V	NO	YES	1μF
LT1133	3	5	+5V	NO	YES	1μF
LT1134	4	4	+5V	NO	YES	1μF
LT1135	5	3	+5V, ±12V	NO	YES	N/A
LT1136	4	5	+5V	YES*	YES	1μF
LT1137	3	5	+5V	YES*	YES	1μF
LT1138	5	3	+5V	YES*	YES	1μF
LT1139	4	4	+5V, +12V	YES*	YES	1μF
LT1140	5	3	+5V, ±12V	YES*	YES	N/A
LT1141	3	5	+5V, ±12V	YES*	YES	N/A
LT1180	**2**	**2**	**+5V**	**YES***	**YES**	**0.1μF**
LT1181	**2**	**2**	**+5V**	**NO**	**YES**	**0.1μF**

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CIRCLE NO 99

Circuit converts pulse height to width

Gordon Anderson
Battelle Northwest, Richland, WA

The output-pulse width from the circuit in **Fig 1** is a linear function of the input pulse's height. You can set the circuit's input threshold to discriminate against low-level pulses, while fixed components limit the circuit's maximum output-pulse width.

With a 270-kΩ resistor connected from the −9V supply to the base lead of Q_2, this circuit can handle input pulses separated by 20 μsec min; without the resistor, input pulses must occur 80 μsec apart for correct operation. The turn-off time of zener diode D_2 sets the lower limit for the input-pulse repetition rate.

IC_1, D_1, and C_3 detect the peak of the input pulse. The comparator, IC_2, triggers at your preset threshold. The RC delay network, R_9 and C_5, hold off inverter IC_3's changing state until the completion of peak detection. After IC_{3A} changes state, Q_1 turns on and then turns on Q_2, a constant-current source.

Constant-current source Q_1 then discharges C_3, the peak-detecting capacitor. When C_3 has discharged below IC_2's threshold, IC_2's output goes low, as do pins 6 and 4 of IC_3. The output-pulse width is a function of this discharge time, which you can adjust with R_6. C_6 and R_7 control the maximum output-pulse width, which is 8 μsec max.

EDN

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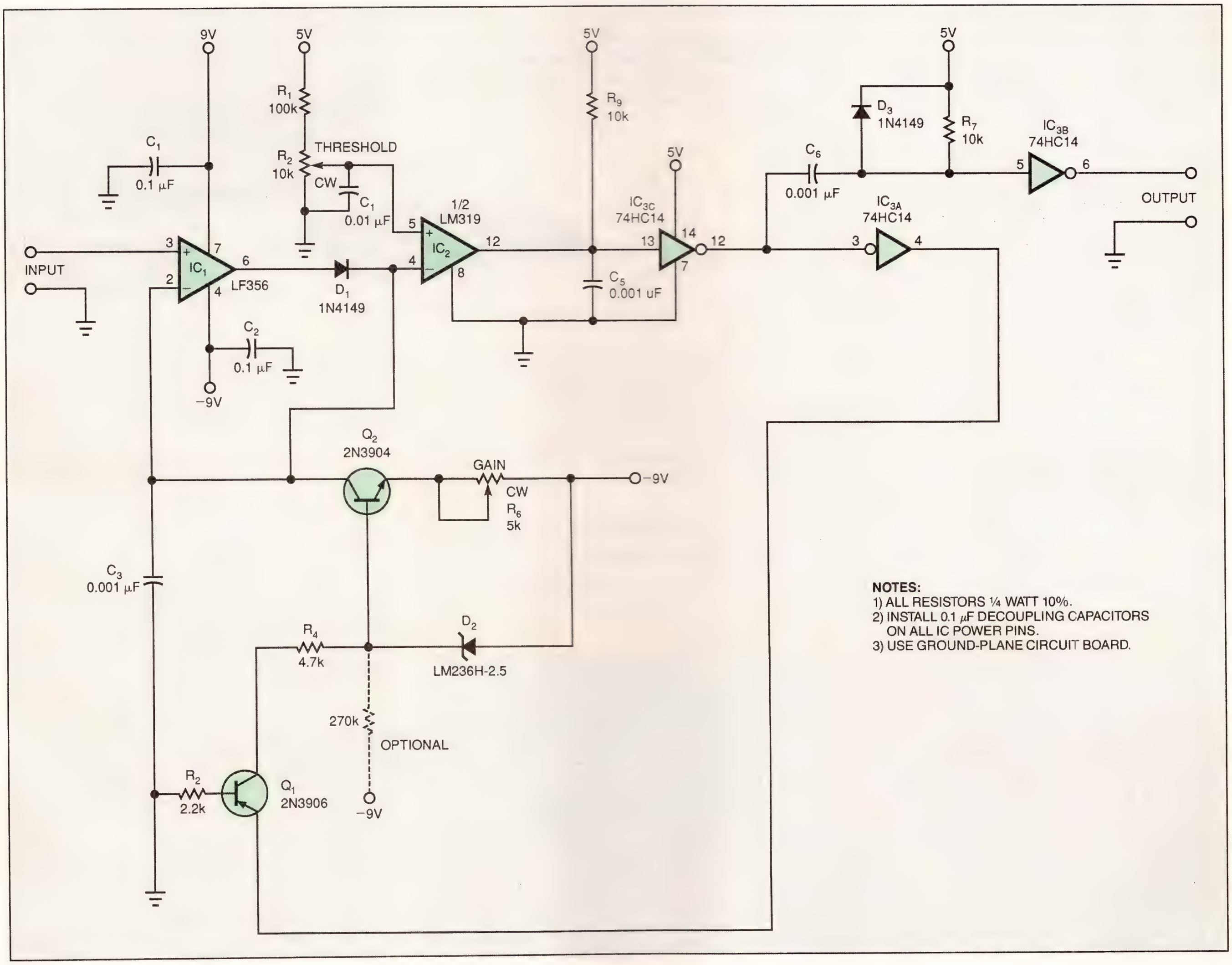

***Fig 1—A peak detector and constant-current** source combine to form a pulse-height to pulse-width converter.*

DRAM tester yields GO/NO-GO information

Dan B Goldish
Raytheon Co, Marlboro, MA

The digital circuit shown in **Fig 1** performs a GO/NO-GO test on a 4164 dynamic RAM (DRAM) by continuously alternating 1s and 0s through the ZIF-socketed unit under test, IC_1. This alternating pattern verifies the integrity of the DRAM's 65,536 data locations, as well as the distinctiveness of each of its 16 address lines. The circuit detects internally shorted address lines and stuck data bits.

Sometime after you apply the reset pulse via SW_1, D_1 will flash to indicate that IC_1 passes the test. D_1 is off during the 0s part of the test and on during the 1s. If the DRAM is faulty, the LED will cease to flash and stay illuminated.

Two 8-bit counters, IC_4 and IC_5, drive IC_1's address lines. The 16R8 controls both counters' enable pins and the $\overline{RAS}$ and $\overline{CAS}$ lines of IC_1. The 74LS590s have two separate clock inputs: a counter clock, CCK, and a register clock, RCK. CCK and RCK are driven from opposite edges. The value of the clock generator is not critical; however, it must be between 768 kHz and 11 MHz, so that the circuit drives the DRAM at the proper speed. A 768-kHz oscillator will meet the minimum $\overline{RAS}$ refresh rate of most 4164 DRAMS, which is 128 rows every 2 msec.

Listing 1 is the Abel source code for the 16R8; **Listing 2** presents the reduced Boolean equations that are programmed into IC_2. The terms SELN, RASN, and CASN form a state machine that enables either IC_5 or IC_4 to drive the multiplexed DRAM address lines. The state machine also controls the low logic levels applied to $\overline{RAS}$ and $\overline{CAS}$. The terms HALF, RWN, and DOUT form a second state machine, which determines the data value to write or read from the DRAM. The term CCKEN is active for one cycle to allow IC_5 to increment at the next row address. Lastly, the term FIRST is used to bypass the initial DRAM read/verify operation until at least one write cycle has transpired

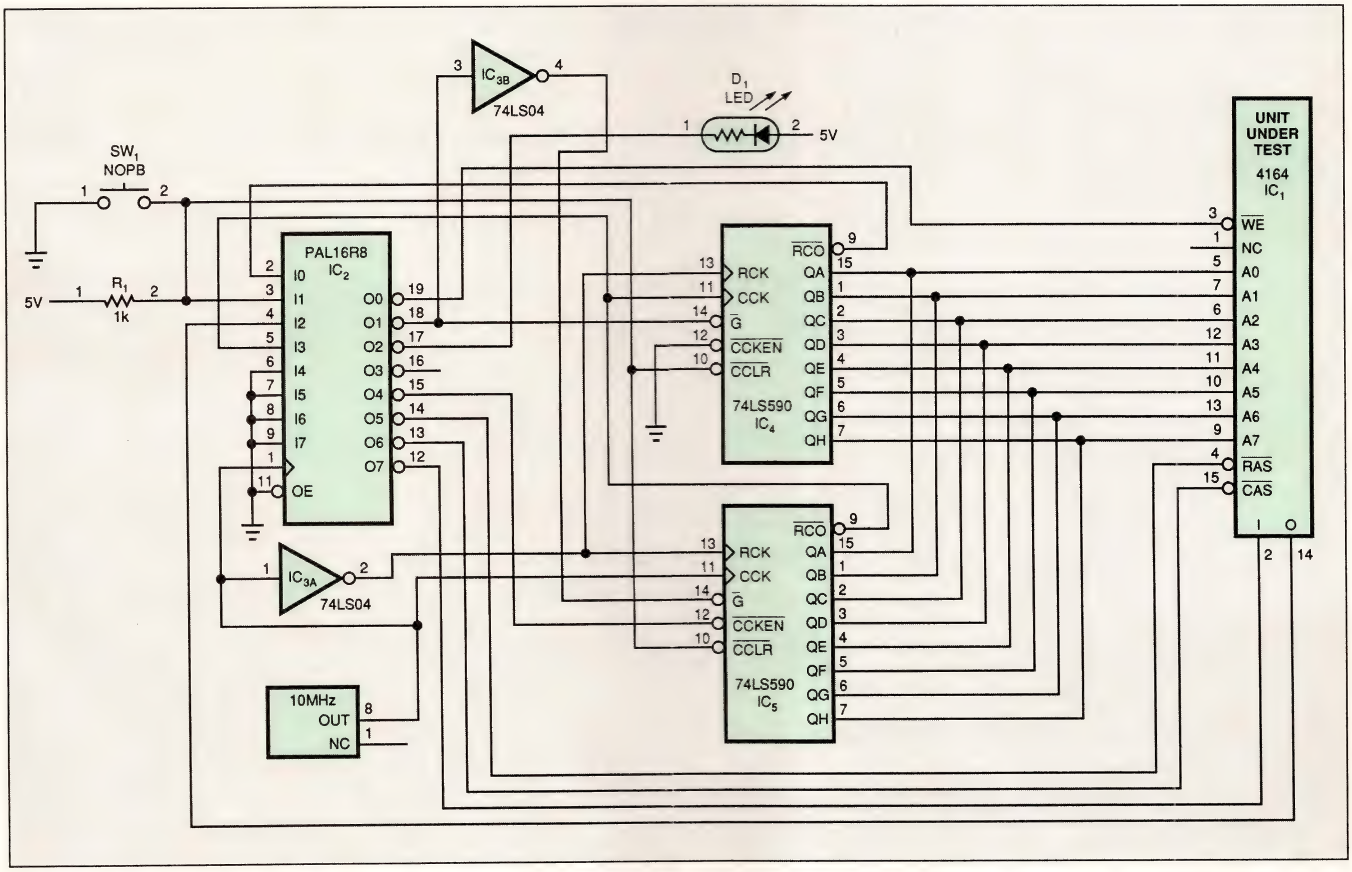

Fig 1—This DRAM test circuit writes 0s and 1s alternately to each data location. A flashing D_1 indicates that the DRAM has passed the GO/NO-GO test.

and valid data is written at each DRAM address.

The procedure consists of reading a single DRAM location and then verifying that the data bit is correct. Next, data of opposite polarity is written to the same address location, and its value is read to verify that the data bit did in fact toggle. If this bit location passes, the next address location is tested in an identical manner. When the 8-bit row address rolls over from FF to 00, the 8-bit column address, IC_4, is incremented via the ripple carry out of IC_5. When both the row and column addresses roll over from FF to 00, the entire DRAM has been tested. The 16R8 then repeats this procedure for the opposite-polarity pattern. Alternate patterns are continuously written and read from the entire DRAM, thus causing D_1 to flash until a DRAM failure. EDN

To Vote For This Design, Circle No 524

LISTING 1—ABEL SOURCE CODE

```
module dram

   flag '-r3', '-t2'

   title 'DRAM Controller for 4164 Chip Tester'

   U2 device 'P16R8';

   CLK pin 1;

   ck = .C.;

   "Inputs
   RCON1,RESETN,DIN,RCON2
   pin 2,3,4,5;

   "Outputs
   RWN,SELN,HALF,FIRST,CCKEN,RASN,CASN,DOUT
   pin 19,18,17,16,15,14,13,12;

   M2 = [HALF,RWN,DOUT];

   M1 = [SELN,RASN,CASN];

   RCO = !RCON1 & !RCON2;

equations

   M2       := [1,1,1] & !RESETN;

   M1       := [1,1,1] & !RESETN;

   !FIRST   := (RCO & (M1==0) & (M2==6)
             #  !FIRST) & RESETN;

   !CCKEN   := (  (M2==6)
             #    (M2==3) ) & (M1==1) & RESETN;

state_diagram M1

   state 7: goto 5;

   state 5: goto 1;
```

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	end, min.	200	400	600	800	1200	1200	1600	1600	1600	1800	2000	2100	2200
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*Prefix P for pins, B for BNC, N for Type N, S for SMA   example: PLP-10.7

C105 REV. E

LISTING 1—ABEL SOURCE CODE *(continued)*

```
        state 1: goto 0;

        state 0: goto 7;


state_diagram M2

        state 7: if CASN then 7
                 else if !FIRST & !DIN then 0
                 else 4;

        state 4: if CASN then 4
                 else 6;

        state 6: if CASN then 6
                 else if DIN then 0
                 else if !RCO then 7
                 else 2;

        state 2: if CASN then 2
                 else if DIN then 0
                 else 1;

        state 1: if CASN then 1
                 else 3;

        state 3: if CASN then 3
                 else if !DIN then 0
                 else if !RCO then 2
                 else 7;

        state 0: goto 0;

    end dram
```

LISTING 2—REDUCED BOOLEAN EQUATIONS

```
HALF := !(!HALF & RCON2 & RESETN
         # !HALF & RCON1 & RESETN
         # !HALF & RESETN & !RWN
         # !DIN & !HALF & RESETN
         # CASN & !HALF & RESETN
         # !CASN & !DOUT & !RCON1 & !RCON2 & RESETN & RWN
         # !CASN & DIN & !DOUT & RESETN & RWN
         # !CASN & !DIN & DOUT & !FIRST & RESETN & RWN);


RWN := !(!CASN & !DIN & !HALF & RESETN & RWN
        # CASN & !HALF & RESETN & !RWN
        # !CASN & !DOUT & !HALF & RESETN
        # CASN & !DOUT & RESETN & !RWN
        # !CASN & DIN & HALF & RESETN & RWN
        # !CASN & DOUT & HALF & RESETN & RWN);


DOUT := !(!CASN & DOUT & RCON2 & RESETN & RWN
         # !CASN & DOUT & RCON1 & RESETN & RWN
```

LISTING 2—REDUCED BOOLEAN EQUATIONS *(continued)*

```
         # !CASN & !DIN & DOUT & RESETN & RWN
         # DIN & !DOUT & RESETN
         # !DOUT & HALF & !RCON1 & !RCON2 & RESETN
         # CASN & !DOUT & RESETN
         # !DOUT & RESETN & !RWN
         # !CASN & DOUT & HALF & RESETN & RWN);


SELN := !(CASN & !RASN & RESETN);

RASN := !(CASN & !RASN & RESETN # CASN & RESETN & SELN);

CASN := !(CASN & !RASN & RESETN & !SELN);

FIRST := !(!FIRST & RESETN
          # !CASN & !DOUT & HALF & !RASN & !RCON1 & !RCON2 & RESETN &
        RWN & !SELN);

CCKEN := !(CASN & DOUT & !HALF & !RASN & RESETN & RWN & !SELN
          # CASN & !DOUT & HALF & !RASN & RESETN & RWN & !SELN);
```

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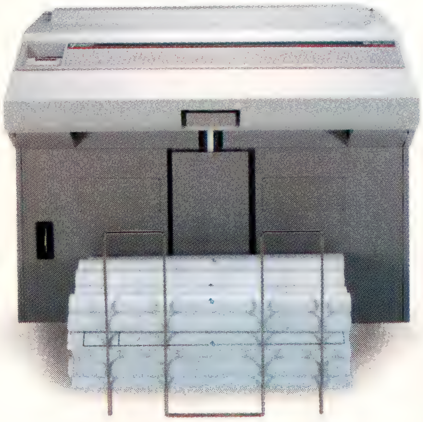

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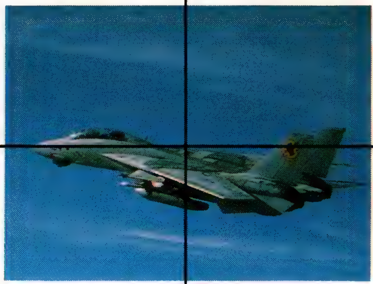

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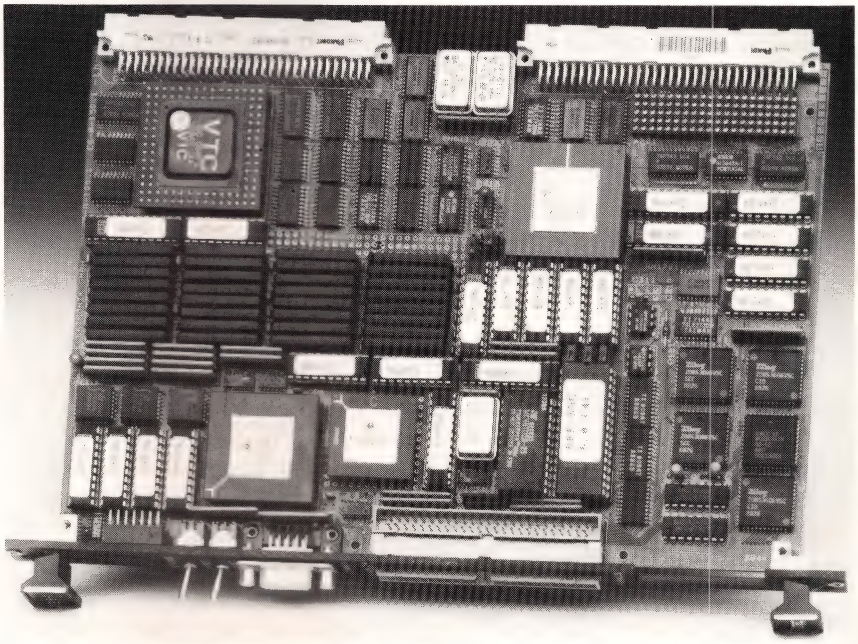
- *Has 20-MHz 68030 μP for VMEbus*
- *Burst-mode access reads cache lines in 280 nsec*

The Eurocom-6, a CPU board for the VMEbus, uses a 20-MHz 68030 μP and has a 68882 coprocessor. A burst-mode access reads complete 4×32-bit cache lines in 280 nsec from its local 8M-byte dynamic RAM. Gate arrays implement VMEbus interface features such as slot one function, master/slave access, interrupt handler and requester, bus arbiter and requester, block mode, and DMA transfer mode. All these features are software programmable. The board also has 256-byte-wide registers that can serve as semaphores to trigger local interrupt requests in multiprocessor applications. Other features include a SCSI interface with a 64k-byte FIFO buffer, four RS-232C ports, a 16-bit parallel port, and six programmable 16-bit timers. Its 2k-byte battery-backed static RAM stores data while the power is off. 20-MHz version, $4500.



American Eltec Inc, 479 S Marengo Ave, Pasadena, CA 91101. Phone (818) 449-1558. FAX 818-578-0054.

Circle No 360

MONITORS

- *Come in 15-in. portrait or 19-in. landscape display formats*
- *15-in. model displays 3300×2560 pixels with 300-dpi density*

The Exact-8000M series comprises two high-resolution, monochrome monitors that come in either 15-in. portrait or 19-in. landscape display formats. Both units display 3300×2560 pixels and have horizontal and vertical pixel densities of 300 and 250 dpi, respectively. Other features include a 750-MHz video bandwidth, a horizontal scan rate of more than 210 kHz, and a noninterlaced refresh rate of 60 Hz. Both units accept analog video inputs, and they have dynamic pin-cushion correction and multipoint dynamic focusing. The yoke handles 15A of defection current when operating at 210 kHz. Instead of a CRT tube, the units use a high-precision electron gun mated with a low-cost glass bulb from Hughes Display Products. Including power supplies, 15-in. model, $2890; 19-in. model, $3690 (OEM qty).

Flanders Research Inc, 88 Bartley Square C-6, Flanders, NJ 07836. Phone (201) 584-0116.

Circle No 361

80386 COMPUTERS

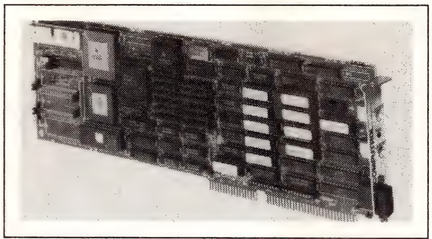
- *Run at 33 MHz and have 64k bytes of cache memory*
- *One 32-bit, six 16-bit, and one 8-bit expansion slot*

The DeskPro 386/33 consists of three models of 33-MHz 80386-based computers. Standard configurations include a 33-MHz 82385 cache-memory controller with 64k bytes of 25-nsec cache memory; a

16-bit integrated video-graphics controller; 2M bytes of 32-bit-wide RAM (expandable to 16M bytes); a parallel port; a serial port; a mouse interface; a 300W power supply; one 32-bit, six 16-bit, and one 8-bit expansion slot; a disk-caching utility; a security lock; and an enhanced 101-key keyboard. Options include a 33-MHz 80387 or Weitek 3167 coprocessor; a 360k-byte or a 1.2M-byte 5¼-in. floppy-disk drive; a 1.44M-byte 3½-in. disk drive; an 84M- to 650M-byte hard-disk drive; a 15-MHz ESDI controller; a 2400-baud modem; a 40M-byte tape drive; and video graphics monitors. Model 84 with 84M-byte drive, $10,499; Model 320 with 320M-byte drive, $14,999; Model 650 with 650M-byte drive, $17,999.

Compaq Computer Corp, 20555 FM 149, Box 692000, Houston, TX. 77269. Phone (713) 370-0670.

Circle No 362



NETWORK CONTROLLER

- *Provides MAP interface for IBM PCs and compatibles*
- *Transfers data at 75,000 bytes/sec between two application levels*

The LP-25 is a Manufacturing Automation Protocol (MAP) network-controller board for IBM PC, PC/XT, PC/AT, and compatible computers. The board and its associated MAP 3.0 software transfer data as fast as 75,000 bytes/sec over a MAP network from one application level to another. Running layers 2 through 7 of the IEEE 802.4 protocol, the board communicates directly to an off-board compatible modem. Using a 12-MHz 68020 µP and an independent DMA controller for data transfers, the LP-25 also features 1M byte of RAM, a 68824 token-bus controller, 512k bytes of EPROM, and a 68091 multifunction peripheral controller. A variety of options support broadband, carrier-band, and fiber-optic networks. Current software packages run with MS-DOS. $2300.

Computrol Inc, 239 Ethan Allen Hwy, Ridgefield, CT 06877. Phone (203) 431-2000. FAX 203-431-2090.

Circle No 363

LAN ACCELERATORS

- *Speed forwarding rates of bridges, gateways, and routers*
- *Have 4096×48-bit content-addressable memory array*

These three IBM PC/AT-compatible boards are hardware accelerators for LAN products. The boards

CIRCLE NO 112

Your ultimate bridge from 1553B to all the computing power you need:

Radstone Mil-Spec VME and Multibus boards.

Now you can connect your 1553 application to high performance, NDI Mil-Spec VMEbus or Multibus computing power. Radstone's 1553 boards are all you need. You can put together a complete Mil-Spec computer system with our supporting processor, memory, I/O and communications boards, ATR chassis and software...for VME or Multibus.

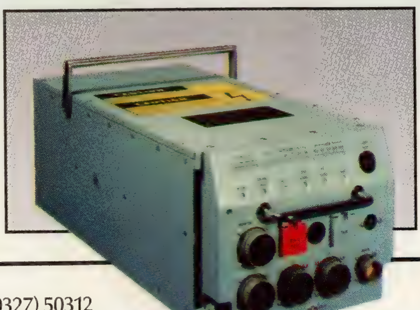
Radstone 1553...full compliance, maximum functionality

Radstone's Mil-Spec 1553B boards serve as the ideal platform to high performance computing. They offer the optimum combination of full compliance with MIL-STD-1553B and either VMEbus or Multibus specs. And they're loaded with the functionality you want for your system, including:

- MIL-STD-1553B dual redundant multiplexed data bus on a single board
- Bus Controller, Remote Terminal and Passive Bus Monitor
- Intelligent interface supported by dual-ported memory
- On-board microcontroller that reduces system overhead
- ATR Chassis and Ada support

Connecting You to Radstone Mil-Spec Products

With Radstone Mil-Spec 1553 boards, you can pass mission critical information to control tactical vehicles such as ships, tanks and aircraft, as well as ground based support facilities. In fact, Radstone 1553 boards are your direct access from the 1553 communications bus to the world's broadest range of full Mil-Spec NDI computer products. Combined with Radstone's other full Mil-Spec computer products, we supply the military exactly what it needs, and we've done so for over 20 years.



Connecting you to Radstone Ruggedized and Commercial Products

In support of tactical applications requiring less than mission critical service, our ruggedized and commercial grade 1553 boards link you to the VMEbus and Multibus on a double Eurocard form factor. Because Radstone's philosophy is to deliver exactly what you need, our supporting processor, memory and I/O boards are also offered in ruggedized and commercial grades.

Hi-Rel Support for Hi-Rel Products

All Radstone 1553 and other Mil-Spec boards are produced in a facility that meets DOD, DEF-STAN and NATO quality standards and are backed by the industry's most knowledgeable and responsive technical support team. Only Radstone brings together the 1553 bus and the power of the VMEbus or Multibus. Call or write for details.

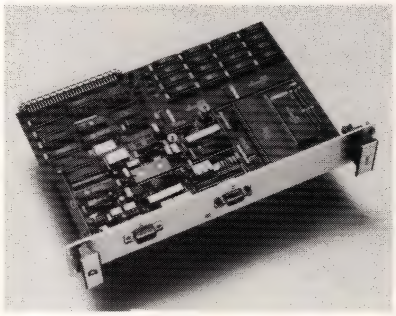
UK Water Lane, Towcester, Northants, NN12 7JN, (0327) 50312
USA 20 Craig Road, Montvale, NJ 07645-1737, (201) 391-2700
France 'Miniparc,' 6 avenue des Andes, 91940 Les Ulis, (1) 64.46.04.03
Germany Bahnhofstraβe 38, D-6090 Rüsselsheim (0 61 42) 6 80 04

RADSTONE
TECHNOLOGY

speed up the forwarding rates of bridges, gateways, and routers. You use the SMC4k-TR accelerator for token-ring LANs and the SMK4k-FD accelerator for Fiber-Distributed Data Interface (FDDI) LANs; the SM4k-GP is a LAN prototyping board. Each board features a content-addressable memory (CAM) array, as large as 4096×48-bits, which stores node addresses. The accelerators can search all of the words in the CAM and compare them with a 48-bit LAN destination address within 100 nsec. The dual-bus configuration consists of a LAN-adapter bus and an IBM PC/AT bus. Menu-driven C software that simplifies the user interface is also available. Board with a 1024×48-bit CAM array, $875; board with 4096×48-bit CAM array, $1625. Delivery, six weeks ARO.

Summit Microsystems Corp, 949 Hillsboro Ave, Sunnyvale, CA 94087. Phone (408) 730-4996.

Circle No 364



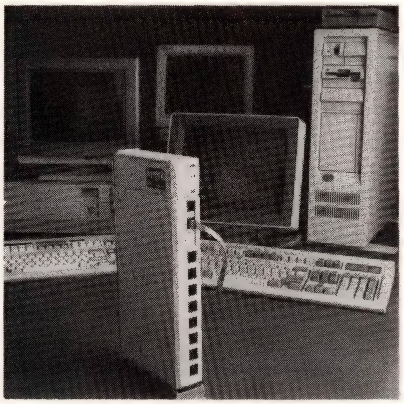
GRAPHICS BOARD

- *Logic for overlaying NTSC video inputs for VMEbus*
- *Uses 63484 ACRTC chip and 512k bytes of onboard memory*

The DGC2 graphics board for VMEbus systems uses Hitachi's 63484 advanced CRT controller (ACRTC), which implements all the graphics control functions. The board contains as much as 512k bytes of graphics memory. The board's logic circuitry allows the ACRTC to be synchronized with an external video signal. The ACRTC output is synchronous with the input image when a decoder oscillator generates the ACRTC pixel-clock frequency. Synchronization essentially stabilizes the image. The board accepts nonmodulated NTSC inputs in the decoder and RS-170 video inputs. Supporting commands for drawing rectangles, polylines, polygons, circles, and ellipses, the board also displays split screens, zooms with 16 to 1 range, and scrolls vertically and horizontally. $2240 (101).

Dynatem Inc, 19 Thomas, Irvine, CA 92718. Phone (714) 855-3235. TWX 910-595-2603.

Circle No 365



CLUSTER CONTROLLER

- *Connects two or more hosts in a StarLAN*
- *Multiple RJ-45 ports that connect to a host 800 ft away*

The MH800 cluster controller connects two or more host computers in a StarLAN configuration. You connect each host on the network to the controller by installing a single StarLAN board in the computer. Each computer can have different operating systems. Twisted-pair telephone-grade wire connects the board to the host as far as 800 ft from the unit. The unit has eight RJ-45 phone jacks for simple snap-on connections. The ports operate simultaneously at 19.2k baud and are programmable from 50 to 38.4k baud. You can expand the LAN to as many as 100 nodes using multiple-cluster-controller connections. The unit has two 16-bit μPs, which offload many of the I/O tasks from the host CPU. 8-port unit for IBM PC/AT hosts, $1495.

Star Gate Technologies Inc, 29300 Aurora Rd, Bentley Park S, Solon, OH 44139. Phone (800) 782-4283. FAX 216-349-2056.

Circle No 366

FRAME GRABBER

- *512×512×8-bit resolution*
- *Accepts RS-170, NTSC, or CCIR monochrome video inputs*

The MV2 frame-grabber board for the IBM PC, PC/XT, PC/AT, and compatible computers accepts RS-170, NTSC, or CCIR monochrome video inputs from interlaced, noninterlaced, or line-scan cameras. A single input channel acquires video data at the real-time speed of 30 frames/sec and digitizes it to 512×512×8-bit frame resolution. Because the image data gets mapped into the I/O space, the host can access the data through I/O read/writes. The board can display an image through its output section or through an IBM VGA-compatible adapter board in the host. The board's output section consists of three 256×8-bit display look-up tables that simultaneously display 256 colors from a palette of 16 million.

Three 15×8-bit overlay look-up tables provide IBM EGA/VGA text and graphics overlays. A complete software library comes with the board. Board and software, $1200.

MetraByte Corp, 440 Myles Standish Blvd, Taunton, MA 02780. Phone (508) 880-3000. FAX 508-880-0179. TLX 503989.

Circle No 367

CARD READERS

- *Low-profile design for smart cards*
- *Contact arrangements meet ISO and CP8 standards*

The Smartcard Reader line of low-profile card readers for smart cards features zero-insertion force, thus minimizing wear. Contact arrangements for the reader meet ISO and CP8 standards. Dual heads and hybrids with both microchip and magnetic-strip readers are available. Card-handling systems include push-push, push-pull, pushmatic with automatic card ejection, push-lift, and push-press with a spring-release card return. The series provides a variety of connectors for flat-cable or flexible-circuit strips. All models pass a 50,000-cycle test. $10 to $35. Delivery, eight to 12 weeks ARO.

Amphenol Industrial Technology Div, Box 4185, Hamden, CT 06514. Phone (203) 287-7300.

Circle No 368

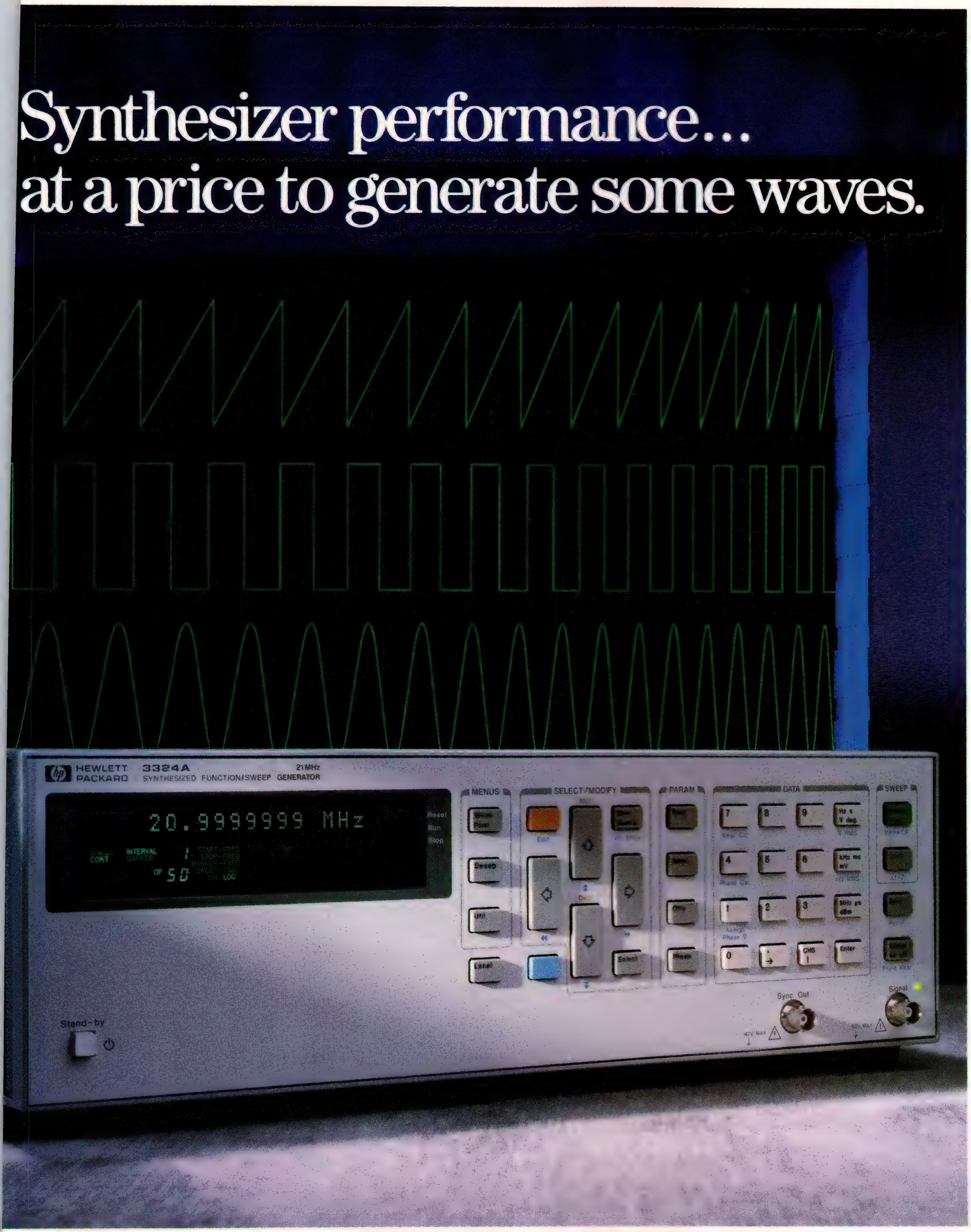
A/D BOARDS

- *10- or 12-bit accuracy digitizing at 20M samples/sec*
- *Daughter board ADC module mounts on 6U VMEbus card*

The ADC10/20M and the ADC12/20M are A/D converters for the VMEbus that can digitize analog data at rates as high as 20M samples/sec with 10- or 12-bit accuracy, respectively. A daughter board ADC module mounts on the reverse side of a 6U VMEbus board. The board also contains a 12-bit DAC that converts data at 20M samples/sec and acts as a system monitor to drive ±1.0V into 50Ω. Besides the analog input, the board can accept 16-bit digital words at 20M words/sec through a front-panel DB25 connector. The board's digital output appears on the P2 connector. Both cards accept analog-input voltages in the range of ±1.0V, and they have 50Ω input terminations. The boards operate from ±15V, 5V, and −5.2V, and dissipate 20W. 10-bit card, $4995; 12-bit card, $9499.

DSP Systems Corp, 1081 N Shepard St, Unit-H, Anaheim, CA 92806. Phone (714) 630-1330. FAX 714-630-6320.

Circle No 369



©1989 Hewlett-Packard Co. TMBID904/F

The new HP 3324A Synthesized Function/ Sweep Generator.

The low price of this new generator is bound to generate some waves. It's much less than you'd expect to pay for a function generator that has 5 ppm frequency accuracy, 9-digit frequency resolution and multi-interval sweep capabilities too.

Put it to work in testing filters and amplifiers where you need synthesizer accuracy, stability and signal purity. Tap its high linearity and multi-interval sweep features for A/D converter testing and for simulating rotating signals. Phase-lock two instruments together to calibrate phase meters and discriminators.

And there's more. Such as the high-stability frequency-reference option, and a high-voltage output option for making really big waves. To find out how low the price really is, call your local sales office today. Ask for our detail-packed brochure and application information.

HEWLETT PACKARD

NEW PRODUCTS

COMPONENTS & POWER SUPPLIES

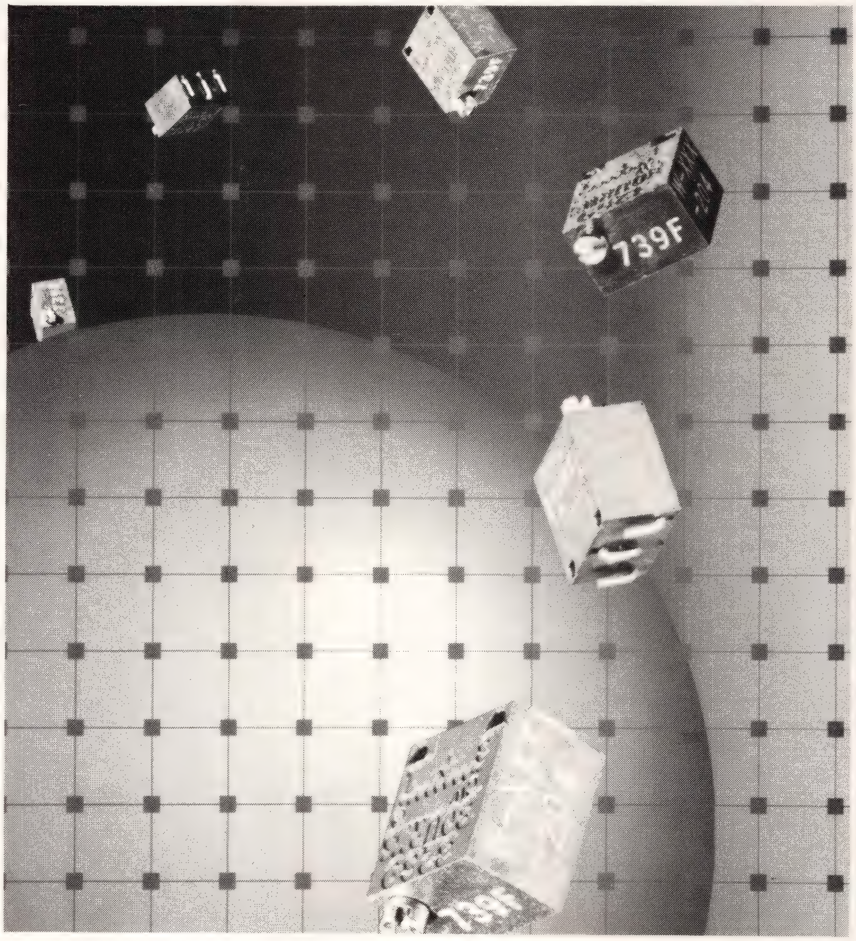
TRIMMER

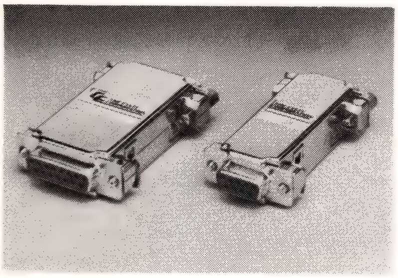
- *Compatible with surface-mount soldering processes*
- *Sealed to accommodate aqueous cleaning techniques*

Measuring 0.25 in. square, the Model 3269 multiturn trimmer is approved per DESC drawing 88040 and meets MIL-R-22097 specifications for nonwirewound variable resistors. The unit is compatible with all popular surface-mount soldering processes. In addition, it is sealed to meet the requirements of high-pressure aqueous cleaning techniques. Standard resistance values range from 10Ω to 1 MΩ. Resistance tolerance is 10%, and resistance contact variation is 3%. The trimmer also features a 250-mW power rating, a 100-ppm/°C temperature coefficient, and a −65 to +150°C operating range. It's available in top- and side-adjust styles. From $1.98 (1000). Delivery, 10 weeks ARO.

Bourns Inc, 1200 Columbia Ave, Riverside, CA 92507. Phone (714) 781-5500. TLX 676423.

Circle No 351





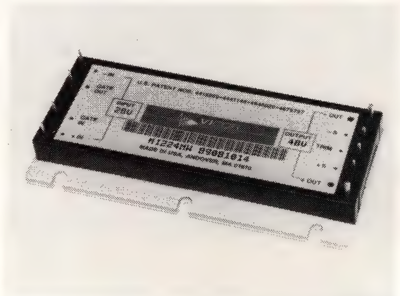
PROTECTORS

- *Provide added security for vulnerable data lines*
- *Feature a 5-nsec clamp time*

The SIP-15M/F(LAN) and SIP-09M/F(LAN) secondary interface protectors enhance the integrity of data transmissions and provide added protection for vulnerable equipment on long cable runs. The -15M/F(LAN) is fully compatible with Ethernet standards; the -09M/F(LAN) accommodates any 9-pin RS-422 or RS-232C interface. Both models are bidirectional and feature a clamping response time of 5 nsec for each protected pin. The -15M/F(LAN) unit protects a total of eight wires—six signal and two power. The -09M/F(LAN) device protects all nine wires, clamping at either 7 or 27V, depending on the application. Each device provides grounding through its respective connector shell. $50 each.

The Cylix Corp, 2637 Townsgate Rd, Suite 200, Westlake Village, CA 91361. Phone (805) 379-3155. FAX 805-378-4551.

Circle No 352

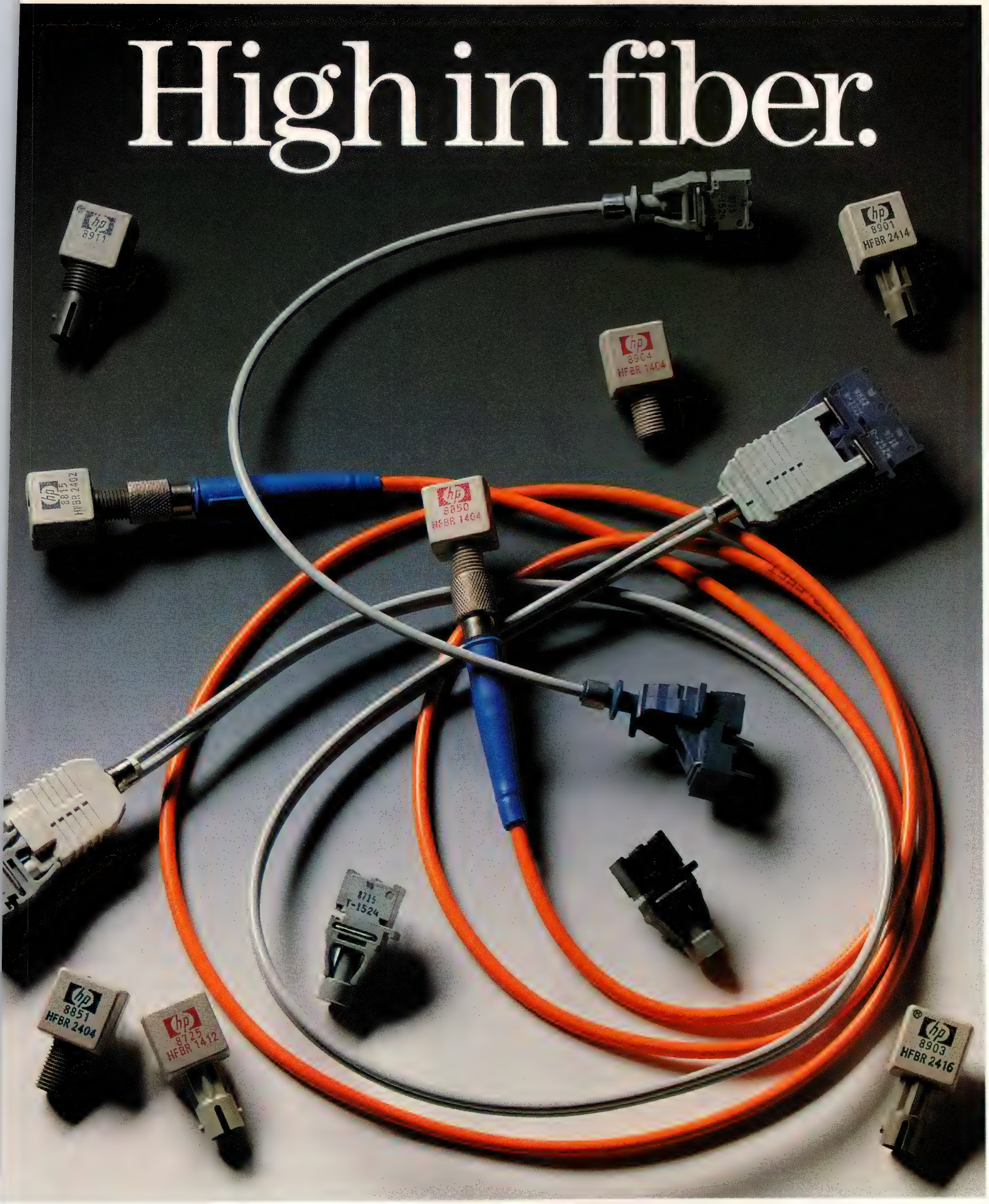


DC/DC CONVERTERS

- *Offer 100W output*
- *Operate to 85°C*

The MI Series military dc/dc converters are available in 28V (MI-220) and 270V (MI-260) versions. The MI-220 units accept 18 to 50V inputs, and the MI-260 models have a 125 to 400V input range. The con-

High in fiber.



At HP, we've got all the fiber-optic components you need. And all at a price that's good for your health.

Our HBFR-0400 family of 820 nm fiber-optic transmitters and receivers provides cost-effective fiber-optic links of up to 4Km. With no assembly time.

The 125 MHz analog receiver is designed for high-speed data links, providing data rates of up to 150MBd. And its wide dynamic range is compatible with the IEEE 802.3 FORIL standard.

The transmitters are specified with four types of fiber and are designed for high-speed transmission, such as with TAXIchip links.

Both the transmitter and receiver are compatible with popular ST and SMA connectors.

HP's HFBR-0501 Versatile Link family includes a complete line of 665 nm fiber-optic transmitters, receivers, connectors and cable. All designed to provide you with a low-cost solution.

Our wide range of plastic cable and connector options includes simplex, duplex, latching and non-latching. Which offers you a cost-effective alternative to copper wire while it provides design flexibility.

Best of all, they're from HP. So you're always assured of HP's commitment to excellence in service, support and reliability.

For a free information package describing our full line of fiber-optic solutions, call **1-800-752-0900, ext. 219R.** It's the best way to get your fiber.

There is a better way.

HEWLETT PACKARD

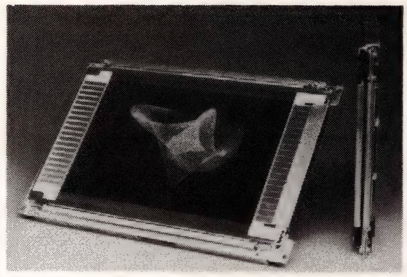
CG 08905

CIRCLE NO 119

verters offer standard outputs of 5, 12, 15, 28, and 48V at 50, 75, and 100W. The units have a power density of 23W/in.^{3}, an 85% efficiency, 3% p-p noise, and a 500,000-hour min life. The converters are rated for full-load operation over −55 to +85°C. All units can be trimmed over a 0 to 110% output range. Overvoltage protection, overtemperature protection, current limiting, remote sense, and inhibit are standard. $540 to $680. Delivery, stock to 10 weeks ARO.

Vicor Corp, 23 Frontage Rd, Andover, MA 01810. Phone (508) 470-2900. FAX 508-475-6715.

Circle No 353



PLASMA DISPLAY

- *Consumes only 35W*
- *Has a 120° min viewing angle*

FPF8050HFUG-A ac memory plasma display carries a Class-B rating—it meets approvals of all UL, FCC, and CSA standards. The 640×400-dot display consumes 35W at full 100% illumination and has a 50,000-hour MTBF. The orange-on-black display features a 120° min viewing angle, a 20:1 contrast ratio, and a character brightness of 44 fL. Complete with driver circuitry mounted directly to the back of the panel, the unit measures just 1.063 in. thick. The viewing area measures 8.3×5.2 in., and the entire panel weighs 2 lbs. $665 (1000).

Fujitsu Component of America, 3330 Scott Blvd, Santa Clara, CA 95054. Phone (408) 562-1000. FAX 408-727-0355.

Circle No 354

POWER SUPPLY

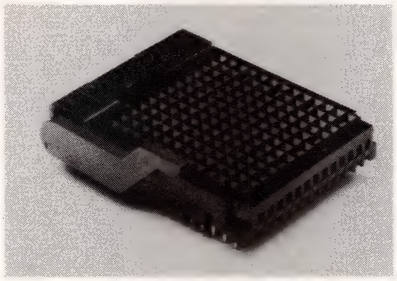
- *Operates in on-line or standby modes*
- *Available in 3-, 5-, and 10-kVA models*

The Topaz Powermaker Mini uninterruptible power supply (UPS) is available with input/output voltages of 120, 208, 220, 230, or 240V ac. Users can select any combination of these values on-site, so one UPS will satisfy applications anywhere in the world. Available in 3-, 5-, and 10-kVA models, the unit can operate on-line or in a standby mode. In the on-line mode, the Mini completely isolates systems from the ac line to provide maximum protection. In standby, the unit has a

4-msec max transfer time. The use of insulated-gate bipolar-transistor (IGBT) PWM technology provides a 300% overload capability. The supply provides a 100-dB common-mode noise attenuation and a 48-dB normal-mode attenuation. It uses sealed lead-acid batteries, which provide 10 minutes of backup time. The batteries are located on two slide-out trays for easy from-the-front installation, servicing, and replacement. $6150 to $14,900.

Square D Co, Power Protection Systems, 9192 Topaz Way, San Diego, CA 92123. Phone (619) 279-0111.

Circle No 355



PGA SOCKETS

- *Feature zero insertion force*
- *Handle arrays as large as 21×21*

Series 650 pin-grid-array (PGA) sockets are zero-insertion-force devices that accommodate arrays ranging from 10×10 to 21×21 pins. The sockets feature normally closed, dual-beam, beryllium-copper contacts. The contacts are plated with 30 μin. of select gold over 50 μin. of nickel. Designed for compatibility with fully automatic loading/unloading operations, the sockets feature a chamfered lead-in area, which eases lead insertion. The socket insulators are made with a thermoplastic material that carries a UL 94V-0 rating. Operating range extends to 150°C. $16.99 (1000) for a 10×10 socket.

Wells Electronics Inc, 1701 S Main St, South Bend, IN 46613. Phone (219) 287-5941.

Circle No 356

VISHAY Electronic Components Group Will Satisfy All Your Resistor Needs

ANGSTROHM

Power Rheostats

MIL-R-22 Approved

Resistance Range from 0.5Ω to 10kΩ

Resistance Tolerance ±10%, others available

Power Rating 12.5, 25, 50, 100, 150 & 300 watts (300°C rise in free air)

Types MP06, MP10, MP15, MP25, MP30, MP40.

Precision Metal Film

MIL-R-10509 & MIL-R-55182 Approved

Over 1.234 billion unit failure rate hours to MIL-R-55182 without a single failure.

Hermetically Sealed Styles RNR/RNN/RNC, Characteristics C & E, Established Reliability.

Resistors, Networks, Specials.

Circle 168

DALE

Precision & Commercial Components Military Trimmers - Techno Division

MIL-R-22097, MIL-R-27208, MIL-R-39015 & MIL-R-39035 Approved

Surface Mounted Components, Wirewound, Metal Oxide & Carbon Film Resistors, Thick & Thin Film Chip Resistors, Resistor & Resistor/Capacitor Networks, Commercial Trimmers, Thermistors, Inductive Components, Transformers, Clock Oscillators, Connectors, Plasma Display, Touch Panels.

Circle 169

ELLIOTT/JORDAN

Precision Wirewound

Temperature Sensing and Compensating, Hermetically-Sealed, Special TCR, Four Terminal, Low Reactance.

Resistors, Printed Circuit, Axial & Radial Leaded, 4 Terminal Molded, Silicone Molded/Coated, Ultra-Miniature, Surface Mount.

Circle 170

OHMTEK

Thin Film

MIL-R-55342 Approved, Char. E, K Chips

TCR to 5ppm/°C

Tracking to 1ppm/°C

Ratio Tolerances to 0.005%

Resistance Range 50Ω to 10MΩ

Precision Custom & Standard Networks SIPs, DIPs, LCCs, Flatpacks, Small Outline Custom Arrays, Silicon & Alumina Chips for Hybrids, Microwave Substrates.

Circle 171

ULTRONIX

Precision & Power Wirewound

MIL-R-26, MIL-R-93, MIL-R-18546, MIL-R-39005 (RBR), MIL-R-39007, MIL-R-39009, MIL-R-55182 & MIL-R-83401 Approved

Established Reliability, Temperature Sensing, Ultra-high Stability, Hermetically Sealed.

Resistors, Printed Circuit, Axial & Radial Leaded, 4 Terminal Molded, Silicone Molded/Coated, Ultra-Miniature, Surface Mount.

Circle 172

VISHAY

Precision Bulk Metal® Foil

MIL-R-122, MIL-R-22097, MIL-R-55182/9 & MIL-R-83401 Approved

TCR to 0.1ppm/°C

TCR Tracking to 0.2ppm/°C

Absolute Initial Resistance to 0.001%

Resistance Ratio Stability to 0.001%

Load Life Stability to 0.0025%

Shelf Life Stability to 0.0005%

Thermal EMF to 0.03V/°C

Resistors, Trimmers, Networks, Chips, Surface Mount, Specials.

Circle 173

VISHAY Electronic Components Group

...a VISHAY Company

63 Lincoln Hwy. ◆ Malvern, PA 19355 ◆ (215) 644-1300 ◆ FAX (215) 296-0657 ◆ Sales FAX (215) 640-9081

PROXIMITY SENSOR

- *Has a 6-in. to 60-ft detection range*
- *Available in a choice of housings*

The ISU-101 proximity sensor, which features a 6-in. to 60-ft sensing range, has a resolution of 0.007 in. and accuracy of ±5%. The sensor is available in plastic or stainless-steel enclosures that are designed to mate with 2-in. NPT fittings for easy mounting in standard fixtures and flanges. The unit offers factory-set or user-programmable detection limits. The sensor can include one or two limit relays and is user programmable using a companion SPU programming unit. Once programmed, the ISU-101 stores its limit settings in permanent memory and operates the internal relays based on these limits. $199.

Contaq Technologies Corp, 15 Main St, Bristol, VT 05443. Phone (802) 453-3332.

Circle No 357

MOTOR DRIVER

- *Drives a choice of motors*
- *Has a 10^6-hour min MTBF*

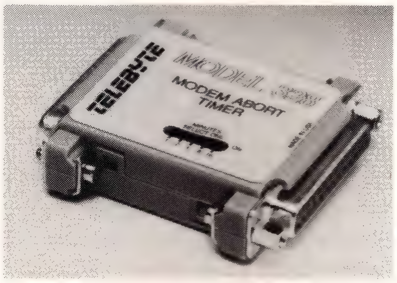
The high-voltage motor driver (HVMD) drives commercially available 220V, 3-phase induction motors or 300V brushless dc motors. It runs directly from a 300V dc bus and can deliver as much as 1 hp. Measuring 2×4×6 in., the HVMD uses an externally generated signal whose 0 to 5V range controls motor speed over a 0 to full rpm range. The driver has a 10^6-hour min MTBF and conforms to IEC 950, UL, TUV, and CSA standards. Other features include a PWM algo-

COMPONENTS & POWER SUPPLIES

rithm during reduced-speed operation, low voltage disable, short-circuit protection, and overload clamp with timed delay shutdown. From $250 (5000).

Cambridge Aeroflo Inc, 900 Mt Laurel Circle, Shirley, MA 01464. Phone (508) 425-2346. FAX 508-425-2338.

Circle No 358



ABORT TIMER

- *Prevents modem tie-up*
- *Features 2-way monitoring*

Model 328 modem abort timer connects between modem and computer ports. It monitors the communications interchange and disconnects the hookup when it detects zero data flow. The timer features a switch-selectable 1- through 16-minute timed interval from initial dial-up to modem abort. It determines whether there has been a transmit data (TD) or a receive data (RD) signal during the timed interval. If it detects no TD or RD signal during the timed interval, the 328 drives the data carrier detect (DCD) signal low for 5 sec. In turn, the host releases the line, freeing the modem to receive new incoming calls. The unit supports synchronous and asynchronous communications and is transparent to full-duplex data and protocol signals. The module comes with male and female DB25 connectors to ease termination procedures. $87.

Telebyte Technology Inc, 270 E Pulaski Rd, Greenlawn, NY 11740. Phone (516) 423-3232. FAX 516-385-8184.

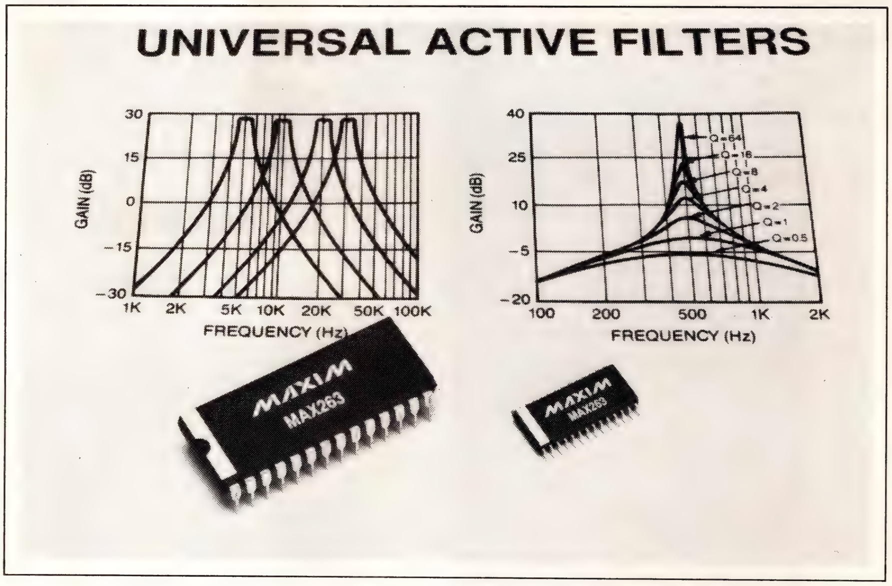
Circle No 359

INTEGRATED CIRCUITS

MONOLITHIC FILTERS

- *Feature pin programmability*
- *Have 0.4-Hz to 140-kHz frequency range*

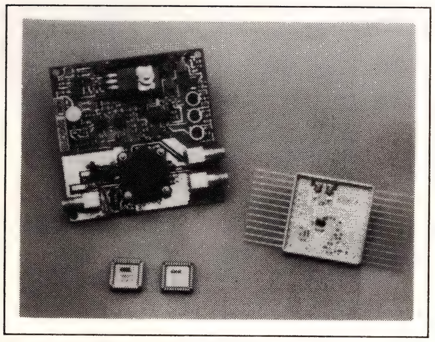
The Max263 and Max264 are pin-programmable, switched-capacitor monolithic filters with center-frequency input ranges from 0.4 Hz to 57 kHz (Max263) and 1.0 Hz to 140 kHz (Max264). Each part has two programmable second-order filter sections, which you can use to implement lowpass, highpass, bandpass, allpass and band-reject filters. Each filter has three outputs (lowpass, bandpass, and highpass/notch) that you can use simultaneously. The center-frequency range is programmed by a 6-bit digital input. The selectivity (Q) for each section is programmed by a 7-bit digital input, which allows a range of Q from 0.5 to 64. The low noise (100 μV rms) of the devices represents



less than ½ LSB in a 12-bit data-acquisition system. PC-based, menu-driven software is available that reduces the design time of nth-order filters to minutes. Both of the filters are available in 24-pin DIPs, ceramic DIPs, and SOIC packages. From $6.50 (1000).

Maxim Integrated Products, 120 San Gabriel Dr, Sunnyvale, CA 94086. Phone (408) 737-7600.

Circle No 370



CLOCK-RECOVERY IC

- *Fabricated in GaAs*
- *Has 50M- to 800M-bps NRZ data rate*

The 16G041-H is a GaAs hybrid circuit that forms a complete PLL clock-recovery and data-retiming/regeneration subsystem. The IC integrates the 16041 clock-and data-recovery monolithic IC with a high-performance loop filter and other components. It can synchronize an internal VCO directly to an incoming digital data stream while simultaneously retiming and regenerating the data stream. The device provides a 50M- to 800M-bps NRZ data rate and comes in a 1.25×1.25-in. surface-mount package. If you want to create a different subsystem, the 16G041 monolithic IC and the 90GCRB demonstration board are available separately. 16G041-H, $247 (100); 16G041, $135 (100); 90GCRB, $845.

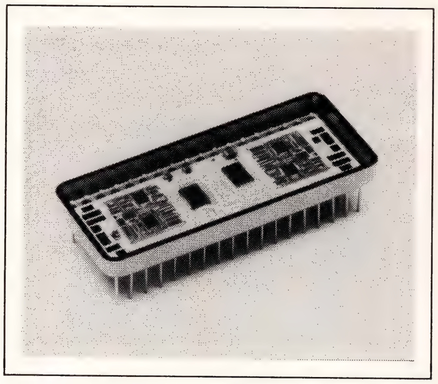
GigaBit Logic, 1908 Oak Terrace Lane, Newbury Park, CA 91320. Phone (805) 499-0610. FAX 805-499-2751.

Circle No 371

D/R CONVERTER

- *16-bit resolution*
- *Pin-programmable gain control*

Packaged in a 36-pin double DIP, the DRC-11522 contains two D/R (digital-to-resolver) converters in one hybrid module. Except for the 16 digital lines, each channel of the DRC-11522 is independent. The module features pin-programmable gain control, 16-bit resolution, an accuracy of ±1 minute, and a scale-factor variation of 0.05%. The mod-



ule also includes a dc-coupled reference and double-latched inputs. With a dc reference input, the DRC-11522 acts as a digital-to-sin/cos dc converter. With the reference input proportional to the radius vector, the device converts polar-to-rectangular coordinates. It operates over −55 to +125°C and is available screened to MIL-STD-883. From $237.

ILC Data Device Corp, 105 Wilbur Pl, Bohemia, NY 11716. Phone (516) 563-5678. FAX 516-567-7358.

Circle No 372

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CIRCLE NO 128

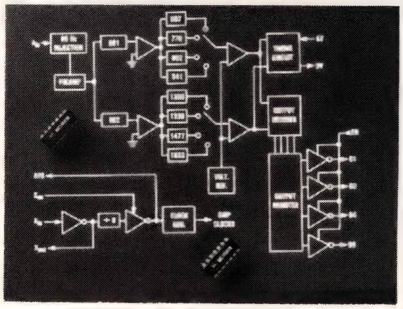
20-PIN PAL-TYPE IC

- *Replaces SSI/MSI logic*
- *Has zero-power capabilities*

Consuming less than 100 μA in the standby mode, the PLC18V8Z-35 logic device is a functional replacement for SSI/MSI logic and a superset of all widely used 20-pin PAL-type devices. The IC's power consumption increases linearly at a rate of 1.5 mA/MHz while in operation. When operating at 20 MHz, the PLC18V8Z consumes less than one-quarter of the power needed by conventional PLA devices. Its universal architecture facilitates combinatorial and sequential (registered) operations. The part has 18 inputs, eight of which are dedicated; you can program each of the eight output macrocells as an input, combinatorial, or registered output, or as a buried register with feedback. The propogation delay of the device is 35 nsec. $3.25 (1000).

Signetics Corp, 811 E Arques Ave, Sunnyvale, CA 94088. Phone (408) 991-2000.

Circle No 373



DTMF RECEIVER

- *Detects all 16 standard digits*
- *Uses inexpensive 3.58-MHz crystal*

The MC145436 DTMF receiver/decoder decodes all 16 standard DTMF tones over −32 to −2 dBm in ISDN applications. The device contains a filter and decoder for detection of tone pairs conforming to the DTMF standard with a 4-bit hexadecimal output code. It has a 3-state output enable and uses a 3.58-MHz crystal or an external clock for timing. Other features include built-in 60-Hz and dial-tone rejection, and guard-time controls to improve speech immunity. The SSI-204 pin-compatible MC145436 comes in a 14-pin DIP. $3.25 (1000).

Motorola Inc, MOS IC Div, Box 6000, Austin, TX 78762. Phone (512) 928-6880.

Circle No 374

S/H AMPLIFIER

- *Features 16-bit accuracy*
- *Has 3.5-μsec acquisition time*

The AD1154 sample-and-hold amplifier maintains 16-bit accuracy in

high-resolution data-acquisition systems at a cost that is 40% lower than competitive devices, according to the manufacturer. The amplifier's guaranteed maximum nonlinearities in sample-and-hold modes is ±0.003 and ±0.00076%, respectively (B grade). Other features include a 3.5-μsec typ (5-μsec max) acquisition time to ±0.00076% of 20V; a 150-psec aperture uncertainty; and an 80-nsec aperture delay. The hybrid IC's 10V/μsec slew rate and its 120-kHz (min) full-power bandwidth provide the range needed in peak-detection circuits. The AD1154 is packaged in a 14-pin metal DIP for use over the −25 to +85°C temperature range, and is available in two grades. A and B grades have maximum hold-mode nonlinearities of ±0.0015 and ±0.00076%, typical acquisition times of 5 and 3.5 μsec, and maximum droop rates of 0.1 and 0.05 μV/μsec, respectively. $42 and $49.50 (100).

Analog Devices Inc, Literature Center, 70 Shawmut Rd, Canton, MA 02021. Phone (617) 461-3532. TLX 924491.

Circle No 375

ANALOG SWITCH

- *Contains eight spst switches*
- *Has ±15V input range*

The DG485 analog switch has a serial input control that lets you connect any combination of the device's eight spst switches to a common output line. The device features a maximum on-resistance of 85Ω and low leakage currents for improved signal accuracy. TTL and CMOS compatible, the DG485 has a switching time (t_{on}) of 200 nsec. The IC operates with either bipolar (±15V) or unipolar (12V) supplies and dissipates less than 105 μW.

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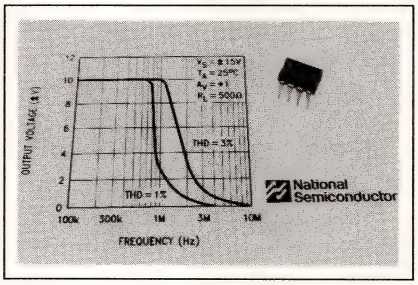
CRITON KORRY

CIRCLE NO 59

It is available in an 18-pin plastic DIP, an 18-pin ceramic DIP, and a 20-pin PLCC package. $6.66 to $7.63 (100).

Siliconix Inc, 2201 Laurelwood Rd, Santa Clara, CA 95054. Phone (408) 988-8000.

Circle No 376



HIGH-SPEED OP AMP

- *Has 400-nsec settling time*
- *Unity-gain bandwidth is 17 MHz*

Manufactured using the company's VIP (vertically integrated pnp) process, the LM6218 dual op amp achieves a 0.01% settling time of 400 nsec. This fast time allows the use of the device in data-acquisition systems that require 12-bit precision. Compared with earlier VIP products, the LM6218 offers a better open-loop gain of 500V/mV and a lower offset voltage of 3 mV. The device's slew rate is 140V/μsec, its unity-gain bandwidth is 17 MHz, and its pnp input stage has a bias current of only 200 nA. It operates over ±5 to ±20V and has a full-power bandwidth of 700 kHz at 1% THD with a ±10V output signal. In an 8-pin DIP, $4.65 (100).

National Semiconductor Corp, Box 58090, Santa Clara, CA 95052. Phone (408) 721-2281. TLX 346353.

Circle No 377

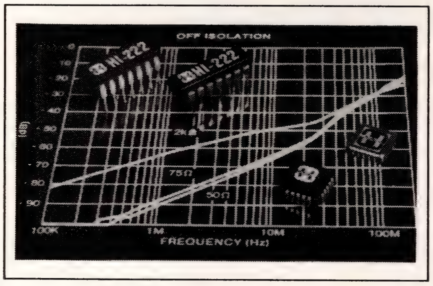
PRECISION OP AMP

- *Offset voltage is 25 μV max*
- *Supply current is 500 μA max*

The LT1012A universal, precision op amp features OP-07A-type performance at lower supply, bias, and offset currents. The device's supply current is 500 μA max, and its bias and offset current are both 100 pA max. Other specs include a maximum offset voltage of 25 μV with a temperature drift of 0.6 μV/°C, a CMRR of 114 dB min, and a PSRR of 114 dB min. The op amp operates at ±1.2V, the equivalent of two NiCd batteries. In 8-pin plastic DIP, $3.95; the reduced-spec LT1012D, $1.60 (100).

Linear Technology Corp, 1630 McCarthy Blvd, Milpitas, CA 95035. Phone (800) 637-5545. FAX 408-434-0507.

Circle No 378



VIDEO SWITCH

- *Operates to 200 MHz*
- *Only 35Ω on-impedance*

The HI-222 high-frequency spst switch has an operating bandwidth that exceeds 200 MHz, and features a 35Ω on-impedance and switching speeds of 100 nsec. The use of dielectric isolation in the fabrication process allows complementary npn-pnp circuit design that provides broadcast-quality differential gain- and phase-error performance of 0.03% and 0.003°, respectively. The TTL-compatible device uses a T-switch design that provides −65-dB off-isolation and −80-dB crosstalk performance at 10 MHz. The HI-222 is available in three temperature ranges and in a variety of package styles, including a 14-pin plastic DIP, a 14-pin ceramic DIP, and a 20-pin PLCC. $4.67 to $21.40 (100).

Harris Semiconductor, Box 883, Melbourne, FL 32901. Phone (407) 724-3800.

Circle No 379

With RadCELL™ 120, it's not a call for help. It's an answer.

Silicon On Sapphire. It's the technology to count on when you're faced with a demand for radiation-hardened performance.

And Rockwell International now gives you easy access to this state-of-the-art capability through a family of CMOS/SOS standard cells.

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RadCELL offers effective channel lengths of just 1.2 microns, achieving one nanosecond gate delay and high density. And you can get the same benefits in VHSIC-compatible CMOS ASICs with Rockwell's MilCELL™ family. In addition, no matter what type of ASICs your project requires, you can depend on Rockwell's Microelectronics Technology Center as a stable source of supply. We've been responding to the special requirements of government programs for more than 20 years.

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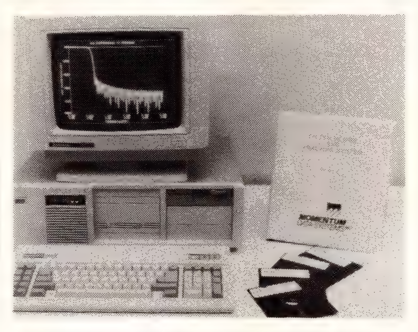
CIRCLE NO 135

CAE & SOFTWARE DEVELOPMENT TOOLS

FILTER-DESIGN TOOL

- *Lets you design and analyze FIR, IIR, and Equiripple filters*
- *Can automatically generate code for 16-or 32-bit DSP chips*

Filter Design and Analysis System (FDAS) 2.0 lets you design FIR (finite impulse response), IIR (infinite impulse response, and Parks McClellan Equiripple FIR filters. The FIR and Parks McClellan packages handle lowpass, highpass, bandpass, bandstop, differentiator, and multiband filters; an FIR filter can have as many as 2048 taps, and a Parks McClellan filter as many as 400 taps. The Parks McClellan package also handles Hilbert transformers and arbitrary-magnitude filters. The IIR package handles lowpass and highpass filters with as many as 40 taps, and bandpass and bandstop filters with as many as 80 taps. The system-analysis package



lets you determine the magnitude, phase, group delay, impulse response, pole/zero locations, and step response of a given transfer function. You can supply the transfer function as a ratio of polynomials, zeros, and poles, or as the product of second-order sections. When you've completed your design, you can invoke a code generator that generates assembly code for AT&T DSP16 or DSP32 processors, or for TI's TMS320 series, or for Motorola's DSP56001 processor. To run the FDAS, you'll need an IBM PC, PS/2, or compatible that is equipped with 640k bytes of RAM, has at least 800k bytes of free hard-disk space, and runs PC-DOS 2.0 or higher. FDAS Version 1 (a subset of the features), $495; FDAS Version 2 (the full set of features), $895; code generators for the DSP16 and DSP32, $200 each.

Momentum Data Systems Inc, 1520 Nutmeg Pl, Suite 108, Costa Mesa, CA 92626. Phone (714) 557-6884. FAX 714-557-6969.

Circle No 380

SECURITY SHELL

- *Protects your computer against viruses*
- *Includes self-test program*

The Integrity Shell is a self-testing command interpreter (shell) for PC-

Text continued on pg 234

...that makes Rantec power supplies FULL-MIL™ qualified.

- **FACT:** DOD is mandating higher standards for solderability, workmanship and construction (MIL-STD-2000 & WS6536).
- **FACT:** Newly revised NAVMAT P4855-1A reflects the military's determined effort to eliminate negligence in power supply design and construction.
- **FACT:** Encapsulation hides inferior commercial practices that corrupt FULL-MIL power supplies (the HALF-a-MIL™ trap).

You really should be able to look inside a power supply to know if it conforms to FULL-MIL specifications. With Rantec FULL-MIL **standard power supplies**, you can easily open the cover– with a screwdriver, not a can opener. You immediately see that the board can be replaced– without dissolving goop and removing wires. Instead you'll find modular construction, with plug-in boards and a separate EMI section. Even I/O connectors are integral parts of the internal assemblies– no wires.

Upon closer examination, you'll see that Rantec FULL-MIL power supplies, as a minimum, utilize JAN-type semi's and established reliability passive components. You'll also see that Rantec military power supplies are fully compliant with MIL-STD-454 for design, workmanship and materials. And you'll certainly appreciate that Rantec FULL-MIL devices are available without lengthy lead times, costly non-recurring engineering charges and other disappointments associated with customs.

Don't be afraid to take a look inside your MIL-SPEC power supply because it's what you can see that makes the device FULL-MIL. Insure power supply reliability and top system performance by specifying Rantec. **Contact us today.**

As a guide to optimizing power in your system design, ask for your FREE copy of "HOW TO SPECIFY FULL-MIL SPEC POWER SUPPLIES: A Guide for Getting Around the Traps of HALF-a-MIL Specifications'.

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9401 Oso Avenue, Chatsworth, CA 91311 ■ TEL: (818) 885-8223 ■ FAX: 8189937780.

CIRCLE NO 138

DOS and MS-DOS computers. The shell works with the standard COMMAND.COM and uses a pseudocryptographic checksum to test each program as DOS loads it. If the checksum computed during loading differs from the checksum that the shell originally embedded in the known-good version, the shell inhibits execution and notifies you that the program has been modified (possibly by a virus). Because Integrity Shell works with, and provides all the facilities of, COMMAND.COM, the shell is totally transparent and cannot cause conflicts with programs of the TSR (terminate-and-stay-resident) type. Another advantage is that the pseudocryptographic checksum is very difficult for a virus to break, and is therefore more secure than the CRC (cyclic redundancy checksum) used by most antiviral programs. $59.95.

MDC Software Inc, Box 10589, State College, PA 16805. Phone (814) 238-7321.

Circle No 381

CASE TOOL

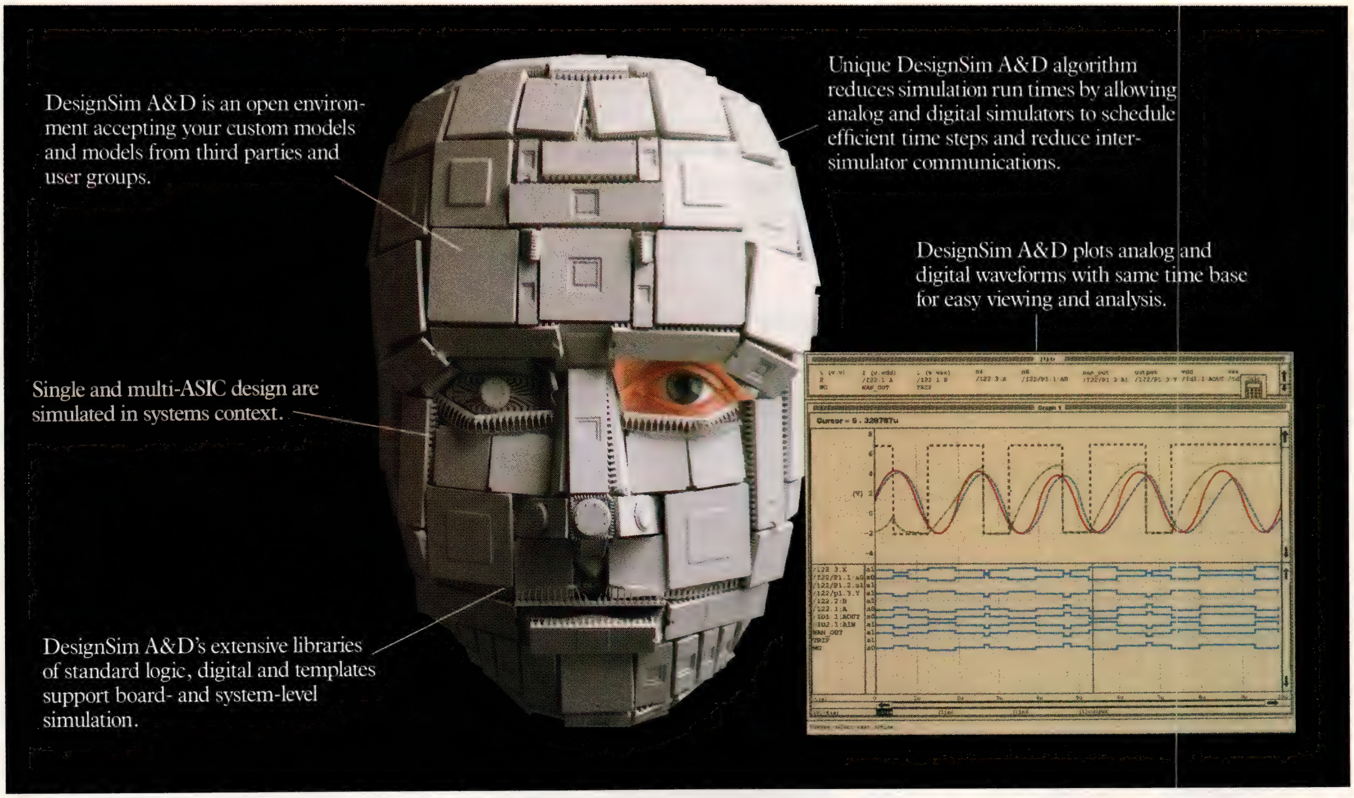
- *Lets you simulate a μC and its environment*
- *Automatically generates MIL-STD documentation*

AutoCode/Matrix$_x$ 2.0 provides all of the functions needed to design and implement the software for an embedded-control system. The package unifies a graphic modeling system with engineering analysis, plotting, simulation, real-time code generation, and automatic documentation facilities. The graphic modeling system lets you design and specify the target system; the simulator lets you simulate the operation of the controller and attached peripheral devices. The analytical features let you perform frequency and stability analysis; linear algebra and equation solving; design optimization; and plotting for data visualization. The code-generation module automatically generates full software code from your completed design. The documentation module automatically generates detailed design documentation that conforms to MIL-STD-2167A requirements and creates hypertext links to requirement and testability information. The package runs on VAX, Sun, or Apollo workstations. $25,000 to $40,000 for a single workstation, depending on the features you want.

Integrated Systems Inc, 2500 Mission Blvd, Santa Clara, CA 95054. Phone (408) 980-1500. FAX 408-980-0400.

Circle No 382

Simulate the real world.



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Your design overwhelms the capabilities of your simulator.

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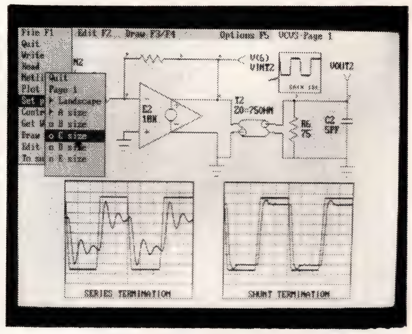
Creating value

NET-LIST GENERATOR

- *Menu-driven graphics editor lets you create analog schematics*
- *Automatically generates Spice-compatible net list*

SpiceNet 2.0 is a graphics editor that runs on IBM PCs, PS/2s, or 80386-based computers and lets you draw and edit analog schematic diagrams using disk-resident symbol, subcircuit, and model libraries. You can create custom symbols at any time and integrate existing compatible artwork and text into your design. The program automatically creates a subcircuit net list, provides automatic pin placement on subcircuit symbols, and lets you



place any Spice primitive or simulation-control directive on the schematic. When you exit from the program, it automatically creates a net list that is compatible with a wide variety of Spice simulators. You can use SpiceNet with the vendor's PreSpice program, which links the net list to models of commonly used devices and components. After running the simulation, the vendor's IntuScope program lets you display the simulation output graphically; you can extract any or all of the waveforms and use SpiceNet again to place the images on your schematic before sending a drawing of the schematic, complete with text, simulated node voltages, and waveforms to a graphics printer or plotter. SpiceNet, \$295; PreSpice, \$200; IS Spice simulator, \$95; IntuScope \$250.

Intusoft, Box 6607, San Pedro, CA 90734. Phone (213) 833-0710.

Circle No 383

CAE TOOLS FOR OS/2

- *Modules include schematic capture, placement, and routing*
- *Modules run under OS/2 and Presentation Manager*

The Ledax Plus tool set, which runs on IBM PS/2s and compatibles, makes use of the Presentation Manager graphical user interface and multitasking features of the OS/2 operating system. The package consists of five tightly coupled modules that share a common database, so that any design changes you make with one tool are automatically re-

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Generations from now, when today's state-of-the-art fighting systems have taken their place in armament history books, today's Abbott power supplies will still be operating reliably.

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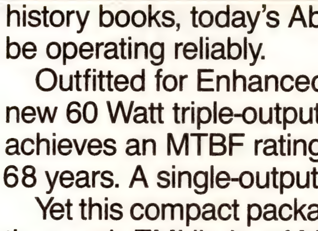
*MTBF FIGURES CALCULATED PER MIL-HDBK-217E GROUND.

Our power supply is built to outlast the tank.



Versatile new 60 Watt switcher measures 5 x 4 x 1.5 inches. Provides outputs of 5, 12, 15, 24 or 28 V dc, from inputs of 18 to 36 V dc. Operating temperature from −55°C to +100°C. Overvoltage protection & short circuit protection standard.

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WHEN RELIABILITY IS IMPERATIVE.™

CIRCLE NO 143

flected in the displays produced by the other tools. The five modules are XScheme, a schematic-capture module; XBoard, a 2-D drafting and documentation tool; XPlace, which performs automatic or interactive component placement; XRoute, which performs automatic or interactive routing; and XPost, an artwork and plotting postprocessor. The tools and database are directly compatible with the vendor's Ledax Power pc-board-design software, which runs on Apollo, Sun, and VAX workstations. $8795.

Microtel Pacific Research Ltd, 8999 Nelson Way, Burnaby, BC, Canada V5A 4B5. Phone (604) 294-1471. FAX 604-293-5787.

Circle No 384

C++ COMPILER

- *Fully compatible with AT&T's release 2.0 of C++*
- *Comes bundled with dbXtra, an enhanced window-based debugger*

The HCR/C++ compiler is 100% compatible with AT&T's Release 2.0 of C++, and comes bundled with dbXtra, an enhanced window-based implementation of the widely used dbx debugger. HCR/C++ provides all the features of AT&T's Release 2.0, such as multiple inheritance, type-safe linkages, and default-membership initialization. Because the compiler translates all C++ code into C before execution, you can use the dbXtra debugger to examine either the original C++ code or the derived C code during debugging. The documentation includes Stroustrup's book *The C++ Language*, together with extensive descriptions of how Release 2.0 differs from the definitions in the book, and full installation and operating instructions. Introductory price, $499.

HCR Corp, 130 Bloor St W, 10th floor, Toronto, Ontario, Canada M5S 1N5. Phone (416) 922-1937. FAX 416-922-8397.

Circle No 385

TRANSLATOR

- *Translates Modula-2 source code to C source code*
- *Runs on PCs or VAX computers*

The M2CC/C translator package consists of three programs and a standard library in the form of definition and object modules. The first program, M2CC, is a single-pass compiler that accepts Modula-2 source code and translates it into processor-independent intermediate code. You can optionally request a list file with integrated error messages. The Modula-2 language definition of M2CC is based on the third, revised edition of Niklaus Wirth's book *Programming*

in Modula-2 (Springer Verlag, Berlin and New York, NY). The second program, M2C, processes the intermediate code and generates a C source file that you can compile to object code using any ANSI-C compiler. M2C processes the intermediate code procedure by procedure and module by module; the output is well structured, and you can integrate standard C libraries into the translated program. The third program, Mak, analyzes a Modula-2 program that consists of multiple compilation units and generates from the program a *make* description file. You can use this description file with the Unix *make* utility to automatically create a consistent program version. PC-DOS version, SFr 1500; VAX/VMS version, SFr 5000.

Glance Ltd, Gewerbestrasse 4, CH-8162 Steinmaur, Switzerland. Phone 01/853-39-49. FAX 01/853-08-09.

Circle No 386

METACOMPILER

- *Runs on IBM PCs, PS/2s, and compatibles*
- *Compiles Forth code to machine code for Harris RTX-2000 μC*

The LMI Forth Metacompiler is a cross-compiler that runs on IBM PCs, PS/2s, and compatibles. The compiler generates native code for the Harris RTX-2000 μC, whose instruction set maps so closely onto essential Forth-language elements that there is no need for an assembler. The metacompiler is a multipass, table-driven translator that allows local labels and conditional compilation directives. It lets you define and invoke new defining words and immediate words in the target code; optionally generates "headerless" code to conserve memory in the target system; and can generate both ROM-resident and RAM-resident code. The metacompiler can even create a new interactive Forth interpreter/compiler that will run on the target system. To run the metacompiler, you'll need a PC, PS/2, or compatible that has at least 320k bytes of RAM and 400k bytes of free hard-disk space, and runs PC-DOS 2.0 or later. You can order it either on two 5¼-in. disks or one 3½-in. microdisk. Other versions of the metacompiler are available for a variety of 8-, 16-, and 32-bit processors from Intel, Motorola, and TI. $750.

Laboratory Microsystems Inc, Box 10430, Marina del Rey, CA 90925. Phone (213) 306-7412. FAX 213-301-0761.

Circle No 387

TEST & MEASUREMENT INSTRUMENTS

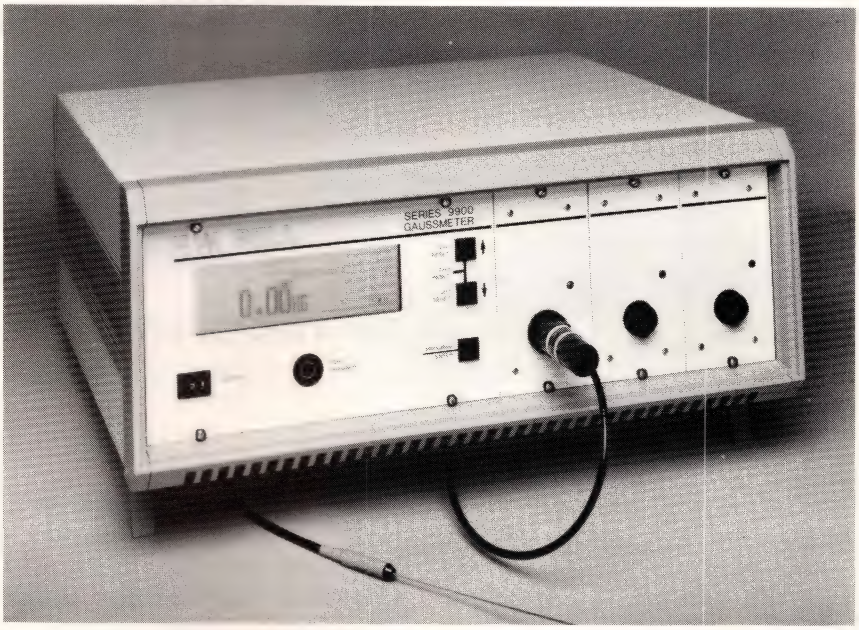
GAUSSMETERS

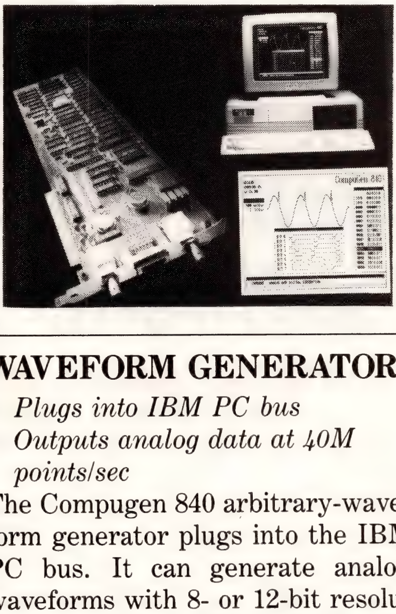
- *Measure 3 to 3M Gauss from dc to 50 kHz*
- *Present data on 4½-digit back-lit LCD*

Gaussmeters in the 9900 Series measure magnetic fields from 3 to 3M Gauss from dc to 50 kHz. The µP-based units, which include both IEEE-488 and RS-232C interfaces, offer a menu-driven user interface and display their results on a 4½-digit back-lit LCD. The vendor offers a full line of probes for the meters. Single-channel unit, $3800. Delivery four to six weeks ARO.

FW Bell Inc, 6120 Hanging Moss Rd, Orlando, FL 32807. Phone (407) 678-6900. FAX 407-677-5765.

Circle No 388





WAVEFORM GENERATOR

- *Plugs into IBM PC bus*
- *Outputs analog data at 40M points/sec*

The Compugen 840 arbitrary-waveform generator plugs into the IBM PC bus. It can generate analog waveforms with 8- or 12-bit resolution. Maximum data rate is 40M points/sec. While generating waveforms with 8-bit resolution, the board can simultaneously produce 8-bit-wide TTL patterns, but such operation restricts the data rate to 20M points/sec (equivalent to 10M 2-state patterns/sec). By sacrificing the waveform-generation capability, you can obtain 16-bit-wide digital patterns or obtain 20M 8-bit-wide patterns/sec. Maximum waveform depth is 16,000 points; maximum digital-pattern depth is 8,000 patterns. The board includes a crystal-controlled timebase, and has trigger capabilities that allow it to produce waveform bursts. The gain of the analog output amplifier is software programmable. $2495.

Gage Applied Sciences Inc, 5905 Saint François Rd, Montreal, Quebec, Canada H4S 1B6. Phone (514) 337-6893. FAX 514-337-8411.

Circle No 389

BOARD-TEST SOFTWARE

- *Adds ability to perform mixed-signal testing*
- *Allows calls to externally compiled programs*

The latest release of software for the vendor's PC-based, 1800 Series of low-cost pc-board testers provides multicolor displays and adds the ability to test mixed signal (analog/digital) boards. The software also allows you to compile programs separately and call them from within a test program. This capability, which permits passing of parameters to the called program, simplifies the use of external instrumentation in test programs. Another added feature is variable timeout of back-drive tests of digital ICs. This feature allows users to safeguard parts that otherwise might be damaged when a back drive condition is prolonged by the occurrence of a fault. A programmable short-circuit-detection threshold allows the use of the tester for inspection of bare pc boards. $1500; testers, $52,250 to $167,160.

Teradyne Inc, 2625 Shadelands Dr, Walnut Creek, CA 94598. Phone (415) 932-6900.

Circle No 390

VOLTAGE STANDARD

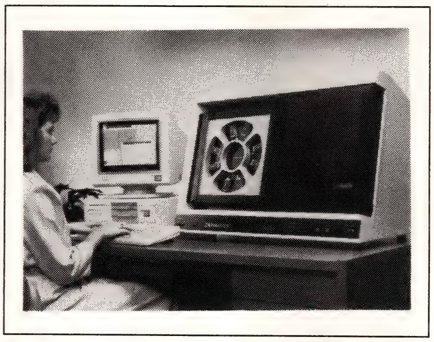
- *Has output stable to better than 1 ppm/year*
- *Includes remote-sensing buffer, which can drive 15 mA*

The 4910 is a solid-state voltage reference whose drift of less than 1 ppm/year rivals that of saturated standard cells. The unit incorporates four 10V "cells," each with its own independent power supply, heater, and temperature-control circuits. Because the elements are independent, errors attributable to

them are uncorrelated and are therefore detectable. The hardware can average the outputs of any combination of the cells to yield an improvement in long-term stability and short-term noise. Each cell incorporates a pulse-width-modulated amplifier, which is inherently stable with both time and temperature. An amplifier with remote sensing and 15-mA drive capability drives the 10V output, making the unit useful without external buffering for calibration of Kelvin-Varley dividers. When you remove ac power, internal batteries continue to supply the reference zener diodes for seven days. For longer periods away from ac sources, the unit accepts 10 to 40V dc standby power. $8995. Delivery, 20 weeks ARO.

Wavetek Corp, Datron Div, Box 85434, San Diego, CA 92138. Phone (619) 450-9971. FAX 619-450-0325.

Circle No 391



ESD TESTER FOR ICs

- *Can test eight 256-pin devices at once*
- *Applies impulses to 8 kV in 50V steps*

The Zapmaster automatic tester verifies the ability of semiconductor devices to withstand ESD pulses whose amplitude is as high as 8 kV. The unit can accommodate eight devices at once, and each device can have as many as 256 pins. The system, which is based on a Compaq 386 computer and runs under the control of MS-Windows-based software, performs V/I curve-trace measurements in 10-nA increments. You can vary the impulse amplitude in 50V steps and set the current rise time from less than 1 to more than 10 nsec. For testing in accordance with MIL-STD-883C, the unit produces a human-body-model waveform with a 5-nsec rise time. $55,480.

Keytek Instrument Corp, 260 Fordham Rd, Wilmington, MA 01887. Phone (508) 658-0880. FAX 508-657-4803.

Circle No 392

POWER ANALYZER

- *Measures V, I, crest factor, power factor, real, and apparent power*
- *Handles 700V, 1000A, and 20 kHz*

The PM1000 precision power analyzer measures the rms value and

10^3

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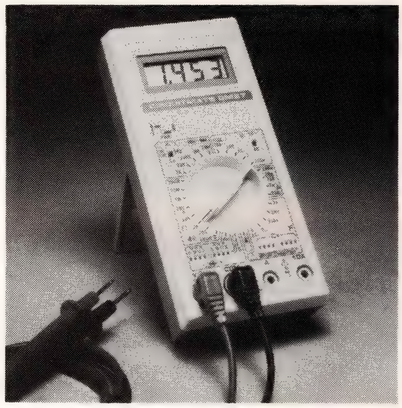
CIRCLE NO 146

harmonic content of voltage and current waveforms. It displays the dc component and the content of odd harmonics through the thirteenth. The instrument also measures real power, apparent power (volt-amperes), power factor, voltage and current crest factors, instantaneous current, and frequency. It handles voltages from 2 to 700V rms, currents from 20 mA to 20A (1000A with an optional current transformer) and frequencies from dc to 20 kHz. $2475.

Voltech Inc, 200 Butterfield Dr, Ashland, MA 01721. Phone (508) 881-7329. FAX 508-879-8669.

Circle No 393



DIGITAL MULTIMETER

- *Measures frequency and capacitance*
- *Checks diodes and LEDs; tests continuity*

The Circuitmate DM27 is a handheld digital multimeter that offers many functions not found in most DMMs. Besides measuring voltage, current, and resistance, the meter measures frequency in five ranges from 2 kHz to 20 MHz and capacitance in five ranges from 2 nF to 20 μF. The meter also audibly checks continuity, tests diodes and LEDs, and incorporates a 20-MHz TTL logic probe that detects 25-nsec-wide pulses. The 11-oz unit, which has a basic dc accuracy of 0.8%, includes test leads, a spare fuse, and a 9V battery. Accessories enable temperature, radio-frequency voltage, high-voltage, and clip-on current measurements. $129.95.

Beckman Industrial Corp, 3883 Ruffin Rd, San Diego, CA 92123. Phone (619) 495-3200. FAX 619-268-0172.

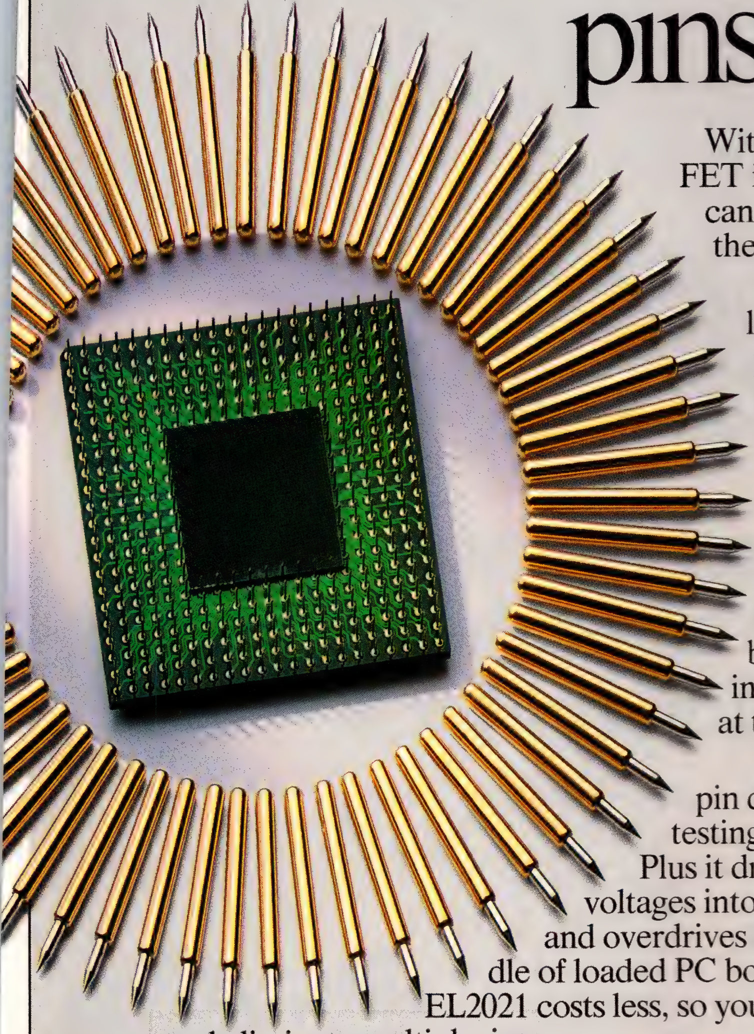
Circle No 394

WAVEFORM RECORDER

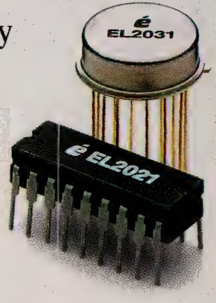
- *Simultaneously captures 12-bit data on four channels*
- *Can take 200k samples/sec on each channel*

The SRA 1204 waveform recorder uses a 12-bit A/D converter on each of its four channels. Each converter can take 200k samples/sec. The

Thanks to Elantec, ATE design engineers are no longer kept waiting on pins and needles.



With Elantec pin drivers and FET input buffers, the ATE industry can stop sitting on the edge of their seats.



Whether it's for IC or loaded PC board testers, our parts are higher performing than the competition. Not to mention more affordable.

As are Elantec analog ICs for all applications—from ATE, video and LANs, to instrumentation, disk drives, and more.

One product that pins down the fastest logic devices is our FET input EL2031 buffer amplifier. It drives 7000V/μs signals into 100 ohm loads. Or buffers those signals at the pin receiver.

Another example is our EL2021 monolithic pin driver. It supports in-circuit and functional testing with a programmable slewrate to 250V/μs. Plus it drives externally programmed voltages into difficult and reactive loads and overdrives device outputs in the middle of loaded PC boards. Best of all, the EL2021 costs less, so you can afford a part per pin and eliminate multiplexing.

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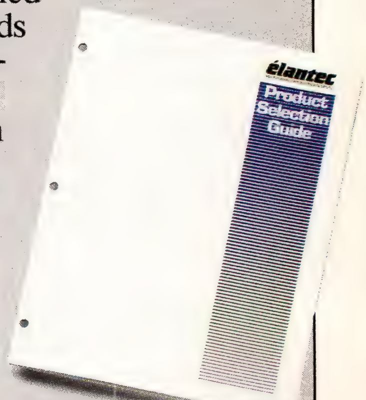

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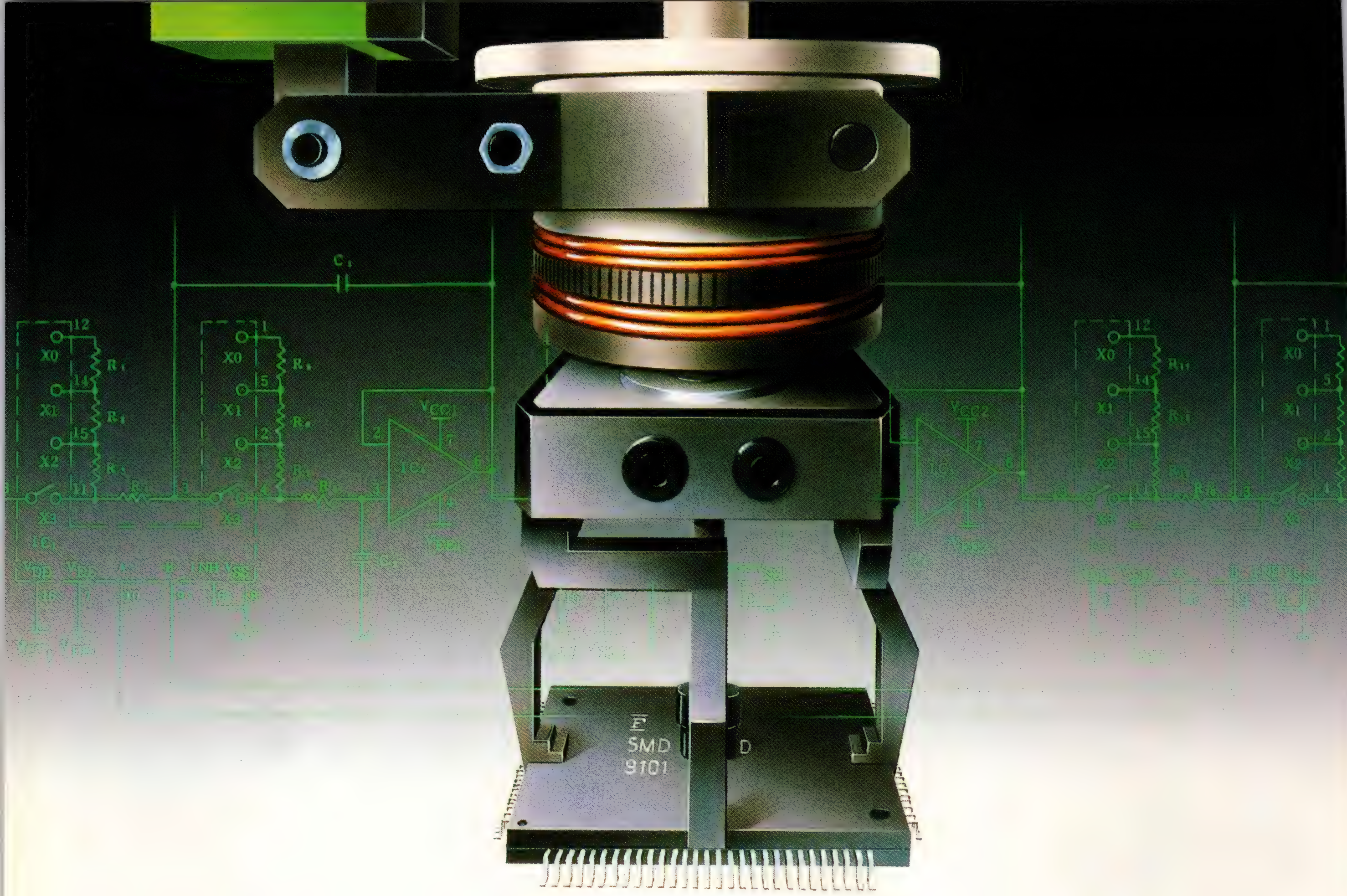

You'll get faster, more precise assembly with Fujitsu SMT hybrid ICs.

Surface-mount technology (SMT) lets you design your products smaller. And produce them faster.

But the range of analog and analog/digital components — amplifiers, filters, comparators and regulators, for example — available in SMT packages has always been very limited. Until now.

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Now you can get the analog, digital and analog/digital hybrid ICs with the specifications you want in the compact SMT formats you need — even circuits with capacitance up to 1μF — or resistance to 10MΩ.

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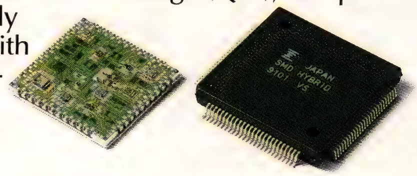
Higher integration, smaller size

Our SMT hybrid ICs are not only precise and reliable, they're also smaller than ever before. Using barechip bonding and double-sided mounting, we've made our Quad Flat Package (QFP), 104-pin SMT hybrid ICs only half the height — with 4 times the integration — of our conventional DIP-type hybrid ICs.



So if you need hybrid ICs in an SMT format, the fastest way to find them is to pick up your telephone. Please call Fujitsu Mikroelektronik GmbH at 069-66320.

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FUJITSU COMPONENT OF AMERICA, INC.:
3330 Scott Blvd., Santa Clara, California 95054-3197, U.S.A. Phone: 408-562-1000 Telex: 910-338-0190 Fax: 408-727-0355
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Telex: 2224361 Fax: (03) 215-1961

FUJITSU

unit, which plugs into the IBM PC bus, includes 64k or 256k words of storage for the sampled data. The board includes a multimode timebase, fast analog trigger, and programmable-gain amplifiers. The vendor bundles the units with a software package called Signal Graphics, which permits interactive control of the host computer and stores data in file formats compatible with third-party data-analysis packages. Also included are software drivers that permit you to create your own customized control software using high-level languages. $2095.

Scientific Recording Assoc, 59 Princeton Terrace, Watertown, CT 06795. Phone (203) 274-7761.

Circle No 395

SIGNATURE ANALYZER

- *Operates at clock rates to 20 MHz*
- *Offers 15-nsec setup time and 5-nsec hold time*

The 20-MHz signature analyzer conforms to accepted signature standards and includes built-in setup routines, self-test routines, and diagnostics. The unit's setup time is 15 nsec; its hold time is 5 nsec. All inputs are fused, and both ac-powered and battery-powered versions are available. For operator training, you can use one unit to simulate fault signatures and a second to trace them. £385.

Flight Electronics, Ascupart St, Southampton SO1 1LU, UK. Phone (0703) 227721. FAX 070-333-0039.

Circle No 396

LOGIC ANALYZER

- *Operates to 100 MHz*
- *Costs under £900 for 32 channels*

The LA3200 is a 32-channel logic analyzer that operates to 100 MHz in synchronous mode and 25 MHz in asynchronous mode. A companion product, the LA4800, offers 48 channels and operates at the same speeds. Instead of CRTs, both units incorporate 640×200-pixel, 9-in. LCDs with fluorescent backlighting; as a result, they are smaller and lighter than most instruments in their speed class. Multilevel triggering provides "If/Then/Else" sequencing and multiple-event or multiple clock-count delays. You can use all of the channels in trigger qualification. The units provide a pair of nonvolatile reference memories and several setup memories. LA3200, £898; LA4800, £1195.

Thurlby Electronics Ltd, Burrel Rd, Saint Ives, Huntingdon, Cambs PE17 4LE, UK. Phone (0480) 63570.

Circle No 397

120-MHz COUNTER

- *Costs less than $700*
- *Optionally includes 1.3-GHz input*

The PM 6662 frequency counter performs reciprocal counting, an unusual capability for an instrument in the under-$700 price class. As a result, the unit provides at least seven digits of resolution with a 1-sec measurement time, even at low frequencies. The basic instrument operates to 120 MHz and provides automatic trigger-level setting. An optional prescaled second channel extends the range to 1.3 GHz. Another option, which holds down the unit's cost, is a mathematically temperature-compensated crystal-controlled timebase (MTCXO). Instead of using a proportional oven, the MTCXO operates the crystal at room temperature, senses that temperature, and mathematically corrects for systematic temperature effects. $645.

John Fluke Mfg Co Inc, Box C9090, Everett, WA 98206. Phone (800) 443-5853, ext 77. TWX 910-445-2943.

Circle No 398

Philips Test and Measurement, Building HKF, 5600 MD Eindoven, The Netherlands. Phone local office.

Circle No 399

WAVEFORM SAMPLERS

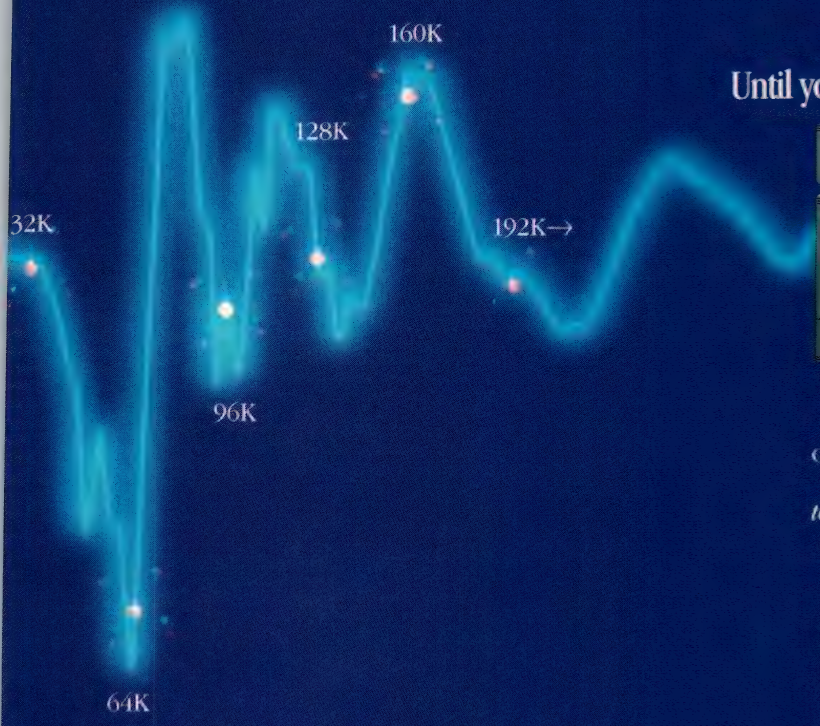
- *Eliminate power divider and associated losses*
- *Limit rms noise to 800 μV max in 12.5-GHz bandwidth*

The SD20 is a single-channel, 20-GHz loop-through sampling head, and the SD22 is a 2-channel low-noise sampling head. Both units plug into the vendor's 11800 Series digital sampling oscilloscopes. The SD20, which features an acquisition rise time of 17.5 psec and typical noise of 1.3 mV rms, eliminates the need for a power divider in high-frequency measurements. Power dividers introduce losses that attenuate the observed signal. The SD22, whose typical rms noise is 400 to 500 μV, and whose maximum rms noise is 800 μV, has a 12.5-GHz bandwidth and an acquisition rise time of 28 psec. SD20, $3250; SD22, $3500.

Tektronix Inc, Box 1700, Beaverton, OR 97077. Phone (800) 835-9433, ext 170.

Circle No 400

You don't know what you've been missing



Until you've seen the new Nicolet 400 Series.

Imagine a memory that expands to 256K—and with four channels, one MegaSample. A unique, removable 44 Megabyte hard disk giving you *ten times* faster data recall and transfer. Time-saving PC interface. MS-DOS, disk downloadable sequences and programs you can customize. Unmatched calculation speed. Easy data archiving. Even four models offering your choice of speed and resolution.

That's the new Nicolet 400 Series. Power. Speed. Flexibility. Convenience. To see what you've been missing in *waveform acquisition,* call or write today.

Nicolet

INSTRUMENTS OF DISCOVERY

Nicolet Test Instruments Division

5225-2 Verona Road, Madison, WI 53711, 608/273-5008 or 800/356-3090

CIRCLE NO 154

Catalog lists test instruments

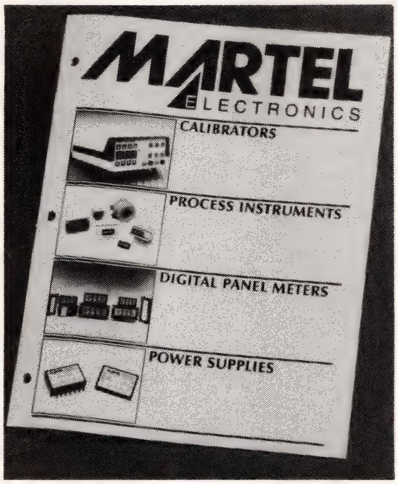
The fall 1989 Heathkit Catalog describes several new models: one benchtop and two handheld and digital multimeters; two assembled oscilloscopes; a clamp meter; and an insulation tester. The publication also gives you information on how to purchase a multimeter.

Heath Co, Dept 350-045, Benton Harbor, MI 49022.

Circle No 401

Booklet features variety of instruments

The vendor's 20-pg instrumentation catalog presents more than 50 products. The publication describes handheld and bench calibrators, more than 20 process instruments, a full line of compact digital panel meters, and linear power supplies.



Product specifications, features, applications, and pricing and ordering information for every product, as well as illustrations, are included in the catalog.

Martel Electronics, Box 897, Windham, NH 03087.

Circle No 402

Presentation of sockets

A 20-pg catalog describes a variety of Textool sockets for test and burn-in applications. The booklet lists sockets for a variety of packages, including DIPs, SIPs, plastic leaded-chip carriers, and leadless ceramic chip carriers.

3M, Dept 89-54, Box 2963, Cedar Rapids, IA 52402.

Circle No 403

Handbook for PC data-acquisition products

The *PC I/O Guide Book*, a "how-to" catalog for PC data acquisition, test, measurement, and control, covers plug-in carrier boards and modules. It also includes a complete software library and guidance for configuring a cost-effective data-acquisition system for IBM PCs, PC/XTs, PC/ATs, and compatible com-

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CIRCLE NO 157

puters; PS/2 model 30; and 386-type computers. The book features the IQ Workstation, the PC Expander, and SuperBoards, as well as the company's line of digital signaling packages.

Intelligent I/O, 1141 W Grant Rd, MS 131, Tucson, AZ 85705.

Circle No 404

RAM-DAC ICs and their uses

Three application notes on video RAM-DAC ICs include waveforms, diagrams, and tables illustrating the use of these DACs. *Video Formats and Required Load Terminations* describes and compares some of the more common standards, and deals with the required load terminations for these DACs. *Improved PCB Layouts for Video RAM-DACs Can Use Either PLCC or DIP Package Types* highlights pc-board layout schemes for the video RAM-DAC portion of an IBM VGA-compatible graphics board. Finally, *Changing Your VGA Design from a 171/176 to an ADV471* explains how an ADV471 is used in a VGA graphics system.

Analog Devices, Literature Center, 70 Shawmut Rd, Canton, MA 02021.

Circle No 405

Manual sums up VMEbus testing

The *CVMEBS1 User Manual* provides the information needed by VME systems designers and integrators to make full use of the CVMEBS1 bus simulator. The publication is divided into six sections, including general information; a hardware-installation guide and operating manual; listings of arbitration and interrupt problems; and a section called "Hints and Kinks," which provides supplementary information for troubleshooting VME systems.

C&C Technology Inc, Bldg 9, Unit 60, 245 W Roosevelt Rd, West Chicago, IL 60185.

Circle No 406

Guide to IEEE-488 products

This 10-pg brochure sums up a comprehensive line of IEEE-488 bus controllers, extenders, expanders, and auxiliary products. The booklet provides photos and product descriptions for more than 40 hardware and software items and accessories.

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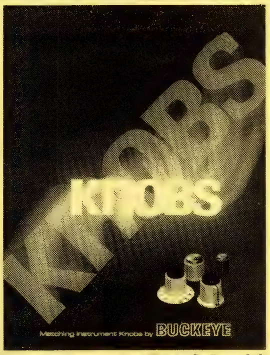

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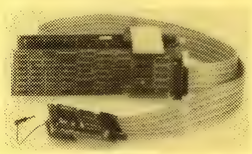

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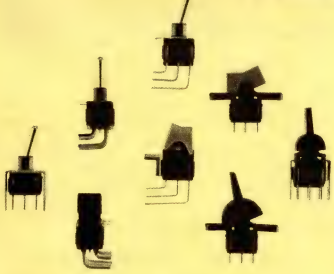

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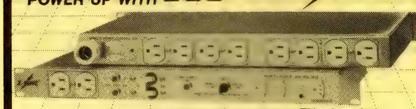

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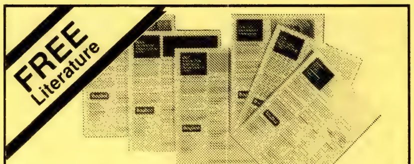

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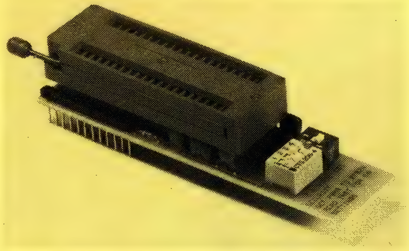

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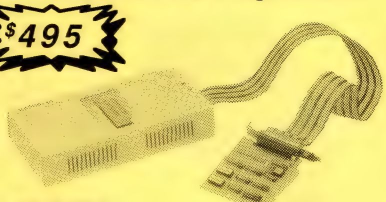

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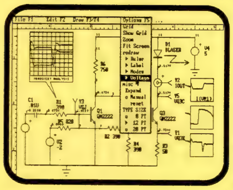

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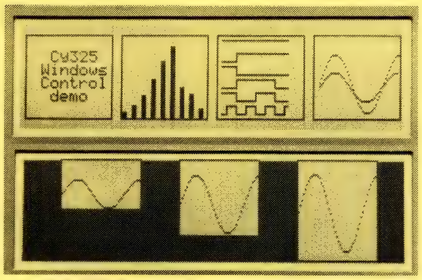

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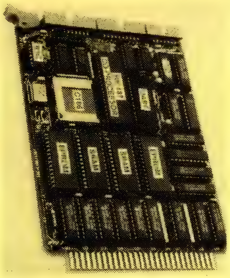

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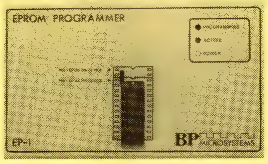

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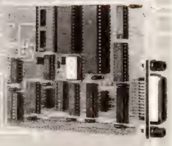

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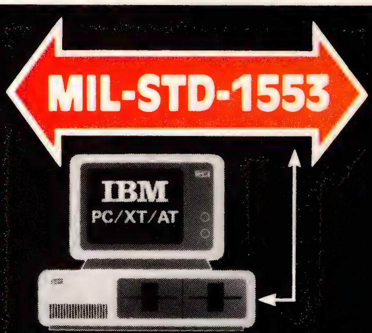

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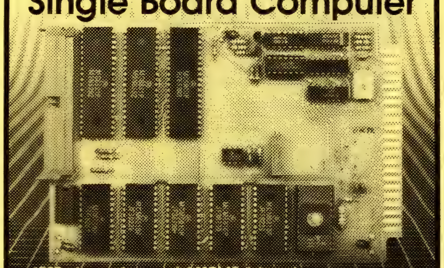

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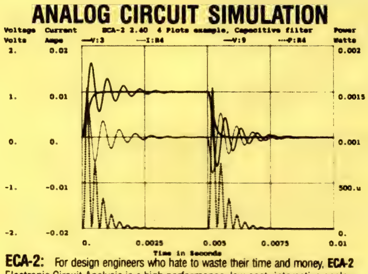

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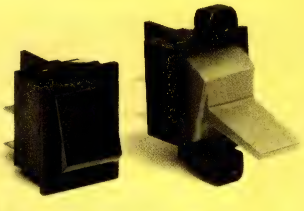

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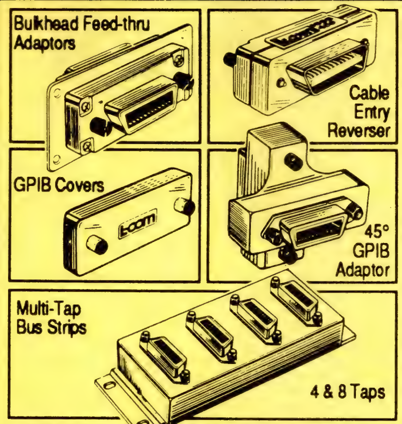

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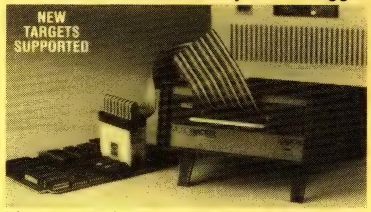

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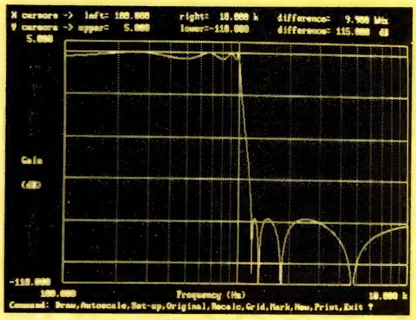

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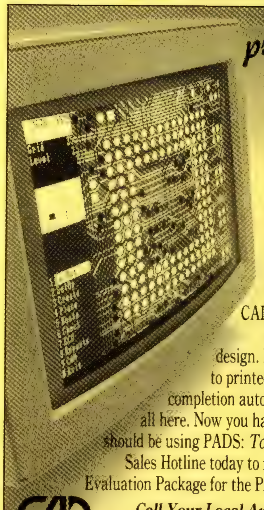

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EDN

Issue Date	Recruitment Deadline	Editorial Emphasis	EDN News Edition
Sept. 14	Aug. 24	Industrial Product Showcase, Digital ICs	Closing: Aug. 30 Mailing: Sept. 21
Sept. 28	Sept. 7	Integrated Circuits, Computer Peripherals	Closing: Sept. 15 Mailing: Oct. 5
Oct. 12	Sept. 21	DSP Chip Directory, Integrated Circuits	Closing: Sept. 28 Mailing: Oct. 19
Oct. 26	Oct. 5	Test & Measurement Special Issue Computers & Peripherals	Closing: Oct. 27 Mailing: Nov. 16
Nov. 9	Oct. 19	CAE, Integrated Circuits	
Nov. 23	Nov. 2	16th Annual μP/μC Directory, Integrated Circuits	Closing: Nov. 9 Mailing: Nov. 30
Dec. 7	Nov. 16	Product Showcase — Volume I, Power Supplies	Closing: Nov. 22 Mailing: Dec. 14
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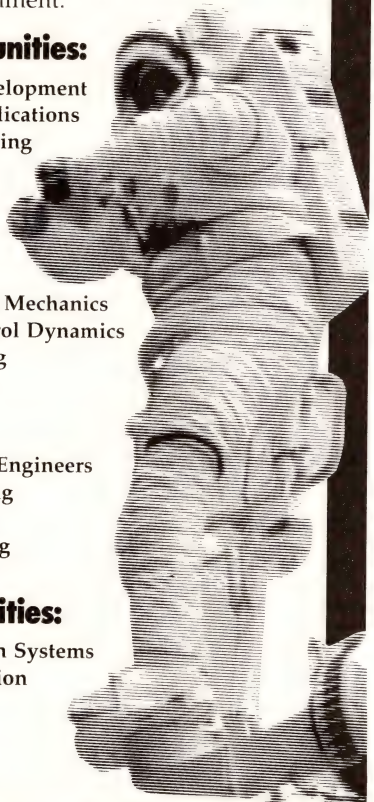

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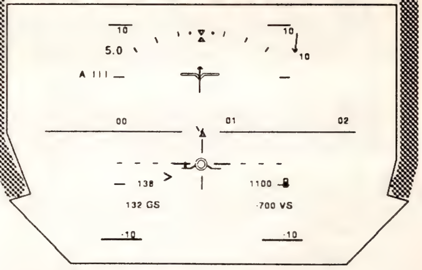

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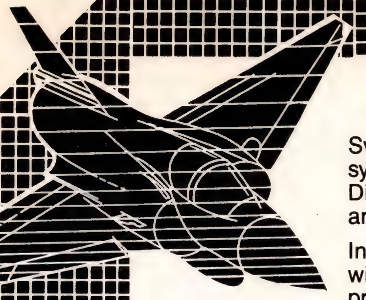

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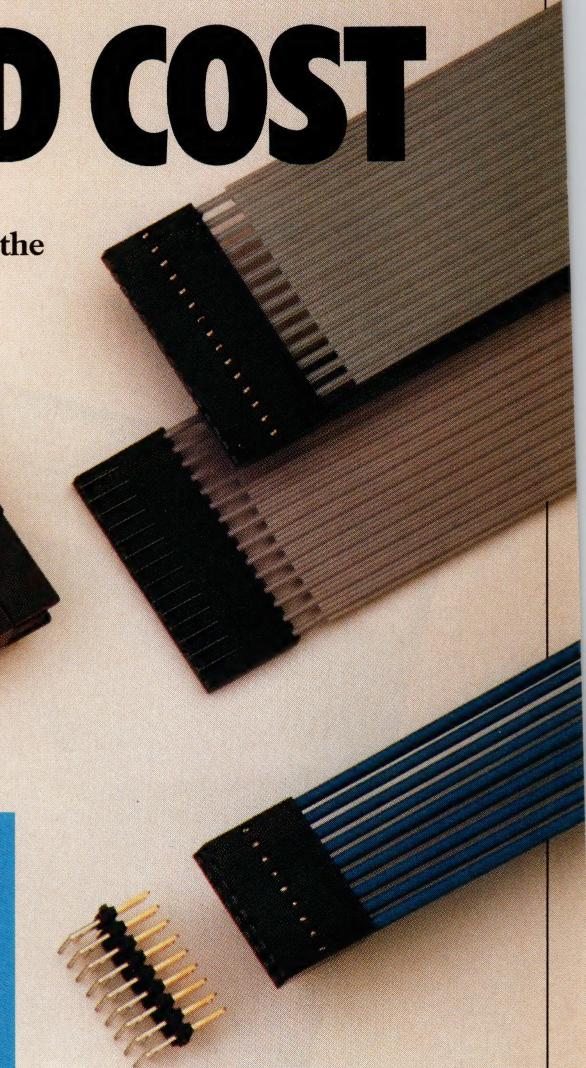

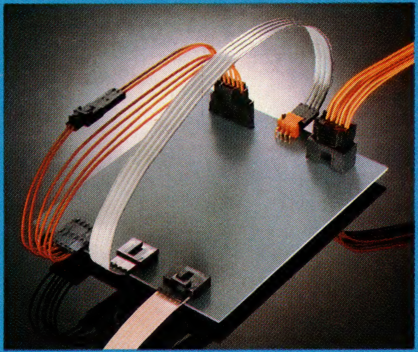

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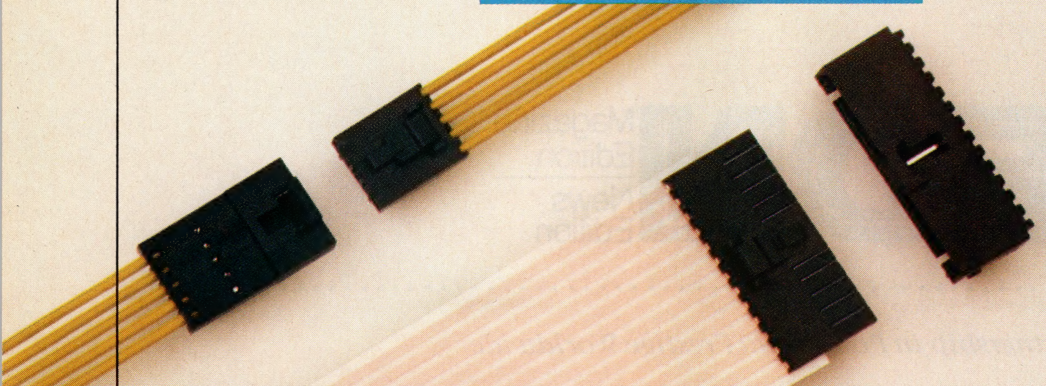

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What's new in chip capacitors?

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Take size. We go small in a big way. Who else can give you chip capacitors as minuscule in size as 1.0mm x 0.5mm.

On the other hand, we've taken capacitor values up—to our highest ever—our GR250 Series and its full 10μF, 16V capacity in an 8.0mm x 6.3mm x 2.7mm package.

We've also developed ways to boost your productivity. Tape packaging, for example, that— using 2mm pitch—gives you twice as many chips on a reel. And bulk chip capacitor magazines that increase the efficiency of auto-placement equipment.

You should know, however, we're still not satisfied —even while shipping 2.5 billion capacitors a month. There's work to be done, more breakthroughs to be made. And we're staying on the job, in traditional Murata Erie style.

So you can remain certain that, when something's new in chip capacitors, you'll hear from us first.

For technical assistance, write or call Murata Erie North America, 1900 West College Avenue, State College, PA 16801, 814-237-1431. For literature or for the location of your local Murata Erie Distributor or Sales office call 1-800-356-7584.

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